FAIRCHILD SEMICONDUCTOR™

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# DM7474
# Dual Positive-Edge-Triggered D-Type Flip-Flops with Preset, Clear and Complementary Outputs

## General Description

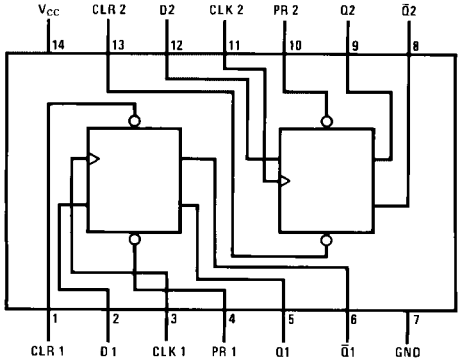
This device contains two independent positive-edge-triggered D-type flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A LOW logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM7474M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| DM7474N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagram




## Function Table

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| PR | CLR | CLK | D | Q | $\overline{Q}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H (Note 1) | H (Note 1) |
| H | H | ↑ | H | H | L |
| H | H | ↑ | L | L | H |
| H | H | L | X | $Q_0$ | $\overline{Q}_0$ |

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going transition of the clock.
$Q_0$ = The output logic level of Q before the indicated input conditions were established.

**Note 1:** This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

## Absolute Maximum Ratings(Note 2)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current | | | | −0.4 | mA |
| $I_{OL}$ | LOW Level Output Current | | | | 16 | mA |
| $f_{CLK}$ | Clock Frequency (Note 4) | | 0 | | 15 | MHz |
| $t_W$ | Pulse Width (Note 4) | Clock HIGH | 30 | | | ns |
| | | Clock LOW | 37 | | | |
| | | Clear LOW | 30 | | | |
| | | Preset LOW | 30 | | | |
| $t_{SU}$ | Input Setup Time (Note 3)(Note 4) | | 20↑ | | | ns |
| $t_H$ | Input Hold Time (Note 3)(Note 4) | | 5↑ | | | ns |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |

**Note 3:** The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

**Note 4:** $T_A = 25°C$ and $V_{CC} = 5V$.

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 5) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max<br>$V_{IL}$ = Max, $V_{IH}$ = Min | | 2.4 | 3.4 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max<br>$V_{IH}$ = Min, $V_{IL}$ = Max | | | 0.2 | 0.4 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 2.4V | D | | | 40 | µA |
| | | | Clock | | | 80 | |
| | | | Clear | | | 120 | |
| | | | Preset | | | 40 | |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max<br>$V_I$ = 0.4V<br>(Note 8) | D | | | −1.6 | mA |
| | | | Clock | | | −3.2 | |
| | | | Clear | | | −3.2 | |
| | | | Preset | | | −1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 6) | | −18 | | −55 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 7) | | | 17 | 30 | mA |

**Note 5:** All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

**Note 6:** Not more than one output should be shorted at a time.

**Note 7:** With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs HIGH in turn. At the time of measurement the clock is grounded.

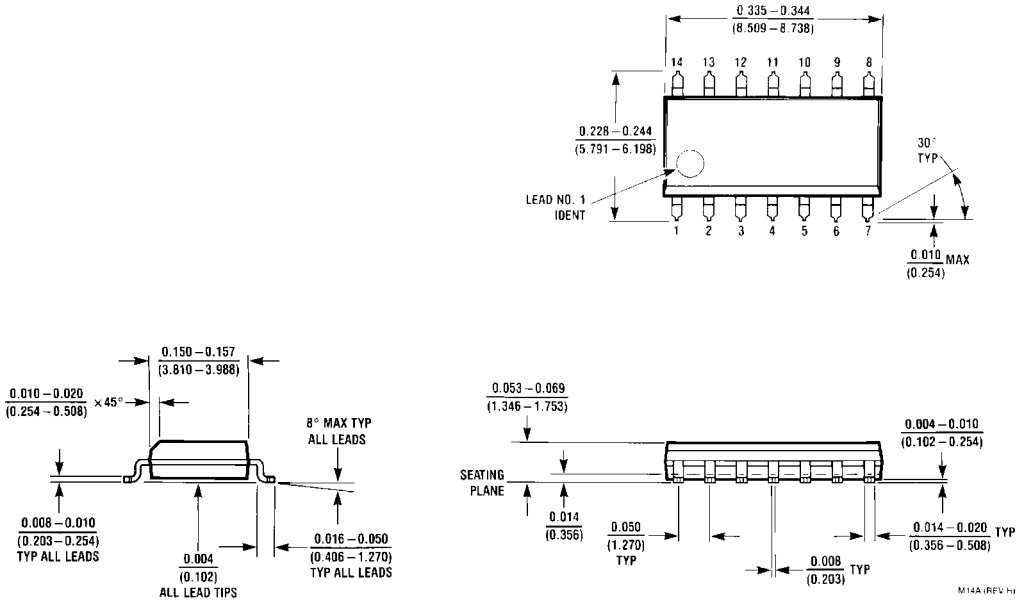
**Note 8:** Clear is tested with preset HIGH and preset is tested with clear HIGH.

## Switching Characteristics

at $V_{CC}$ = 5V and $T_A$ = 25°C

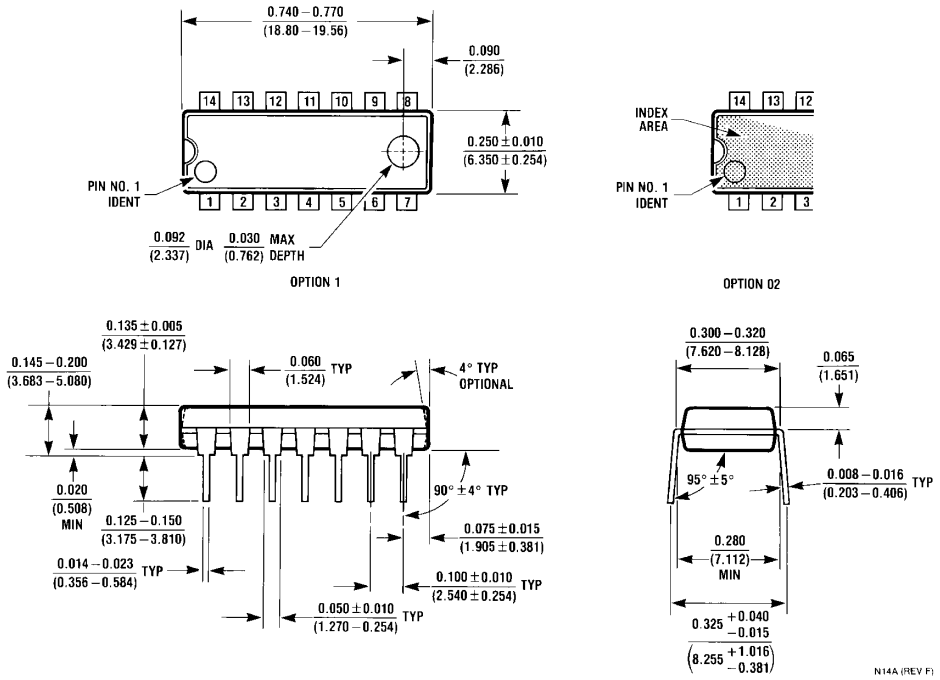
| Symbol | Parameter | From (Input) To (Output) | $R_L$ = 400Ω, $C_L$ = 15 pF | | Units |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | | 15 | | MHz |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Preset to $\overline{Q}$ | | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Preset to Q | | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clear to Q | | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Clear to $\overline{Q}$ | | 25 | ns |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Level Output | Clock to Q or $\overline{Q}$ | | 40 | ns |
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Level Output | Clock to Q or $\overline{Q}$ | | 25 | ns |

## Physical Dimensions inches (millimeters) unless otherwise noted




**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M14A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N14A**