27 GHz to 32 GHz, GaAs, pHEMT, MMIC Power Amplifier

Data Sheet **HMC1132PM5E**

FEATURES

- P_{SAT}: 29.5 dBm
- High output IP3: 37 dBm
- High gain: 24 dB (typical) at 29 GHz to 32 GHz
- DC supply: 5 V at 650 mA
- 50 Ω matched input/output
- 32-lead, 5 mm × 5 mm LFCSP package: 25 mm^2

APPLICATIONS

- Point to point radios
- Point to multipoint radios
- Very small aperture terminals (VSATs) and satellite communication (SATCOM)
- Military and space

FUNCTIONAL BLOCK DIAGRAM

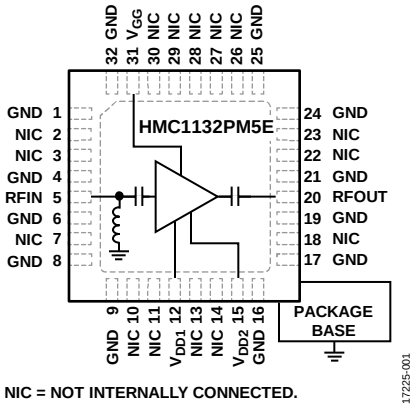

Figure 1.

GENERAL DESCRIPTION

The HMC1132PM5E is a four-stage, gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC) power amplifier. The device operates from 27 GHz to 32 GHz, providing 24 dB of gain and 29.5 dBm of saturated output power from a 5 V power supply.

The HMC1132PM5E exhibits excellent linearity with high output third-order intercept (IP3) of 37 dBm, and it is optimized for high capacity, point to point and point to multipoint radio systems. The amplifier configuration and high gain make the HMC1132PM5E an ideal candidate for last stage signal amplification before the antenna.

The HMC1132PM5E amplifier input/outputs (I/Os) are internally matched to 50 Ω. The device is housed in a RoHS compliant, premolded cavity, 5 mm × 5 mm LFCSP package, making the device compatible with high volume surface-mount technology (SMT) assembly equipment.

Rev. 0 Document Feedback

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REVISION HISTORY

9/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD1} = V_{DD2} = 5 V, quiescent current (I_{DDQ}) = 650 mA, and frequency range = 27 GHz to 29 GHz, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		27		29	GHz	
GAIN		19	22		dB	
Gain Variation over Temperature			0.028		dB/°C	
RETURN LOSS						
Input			7		dB	
Output			9		dB	
POWER						
Output Power for 1 dB Compression	P1dB	26.5	28.5		dBm	
Saturated Output Power	P_{SAT}		29.5		dBm	
OUTPUT THIRD-ORDER INTERCEPT	IP3		37		dBm	Measurement taken at 5 V, 650 mA, output power (P_{OUT}) per tone = 20 dBm
NOISE FIGURE	NF		7		dB	
SUPPLY VOLTAGE	V_{DD}	4		6	V	
QUIESCENT SUPPLY CURRENT	I_{DDQ}	500		750	mA	Adjust the gate bias voltage (V_{GG}) from −2 V up to 0 V to achieve desired quiescent current (I_{DDQ})

T_A = 25°C, V_{DD1} = V_{DD2} = 5 V, quiescent current (I_{DDQ}) = 650 mA, and frequency range = 29 GHz to 32 GHz, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		29		32	GHz	
GAIN		21	24		dB	
Gain Variation over Temperature			0.034		dB/°C	
RETURN LOSS						
Input			11		dB	
Output			14		dB	
POWER						
Output Power for 1 dB Compression	P1dB	27	29		dBm	
Saturated Output Power	P_{SAT}		29.5		dBm	
OUTPUT THIRD-ORDER INTERCEPT	IP3		37		dBm	Measurement taken at 5 V, 650 mA, P_{OUT} per tone = 20 dBm
NOISE FIGURE	NF		5.5		dB	
SUPPLY VOLTAGE	V_{DD}	4		6	V	
QUIESCENT SUPPLY CURRENT	I_{DDQ}	500		750	mA	Adjust the gate bias voltage (V_{GG}) from −2 V up to 0 V to achieve desired quiescent current (I_{DDQ})

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Bias Voltage (V_{DDx})	6.5 V
Gate Voltage (V_{GG})	−2.5 V to +0.5 V
Radio Frequency Input Power (RFIN)[1]	18 dBm
Continuous Power Dissipation (P_{DISS}), T_{BASE}[2] = 85°C (Derate 57.47 mW/°C Above 85°C)	5.17 W
Output Load Voltage Standing Wave Ratio (VSWR)	7:1
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C
Peak Reflow Temperature, Moisture Sensitivity Level 3 (MSL3)[3]	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	Class 0B, passed 150 V
Junction Temperature to Maintain 1 Million Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction Temperature (T_{BASE}[2] = 85°C, V_{DDx} = 5 V)	141.55°C

[1] Maximum input power is limited to 18 dBm or thermal limits constrained by maximum power dissipation (see Figure 31), whichever is lower.

[2] T_{BASE} is the actual temperature on the package base.

[3] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package	θ_{JC}	Unit
CG-32-2[1]	17.4	°C/W

[1] Thermal resistance (θ_{JC}) was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground paddle, to the PCB, and the ground paddle is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

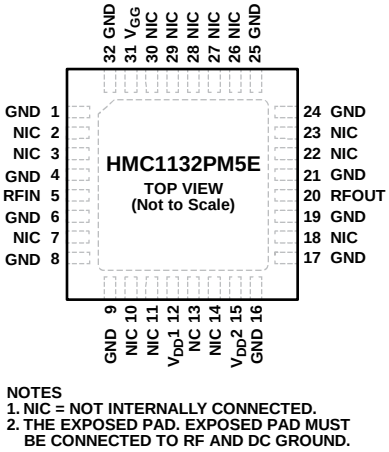


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6, 8, 9, 16, 17, 19, 21, 24, 25, 32	GND	Ground. These pins and the exposed pad must be connected to RF and dc ground.
2, 3, 7, 10, 11, 13, 14, 18, 22, 23, 26 to 30	NIC	Not Internally Connected. These pins are not connected internally. However, all data was measured with these pins connected to RF and dc ground externally.
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 4 for the RFIN interface schematic.
12, 15	V_{DD1}, V_{DD2}	Drain Bias Voltage. External 100 pF, 10 nF, and 4.7 µF bypass capacitors are required. See Figure 5 for the V_{DD1} and V_{DD2} interface schematic.
20	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.
31	V_{GG}	Gate Control for Amplifier. Adjust V_{GG} to achieve the recommended bias current. External 100 pF, 10 nF, and 4.7 µF bypass capacitors are required. See Figure 7 for the V_{GG} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface

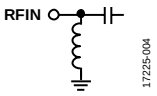


Figure 4. RFIN Interface

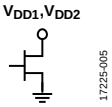


Figure 5. V_{DD1} and V_{DD2} Interface

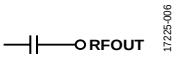


Figure 6. RFOUT Interface

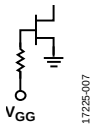


Figure 7. V_{GG} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

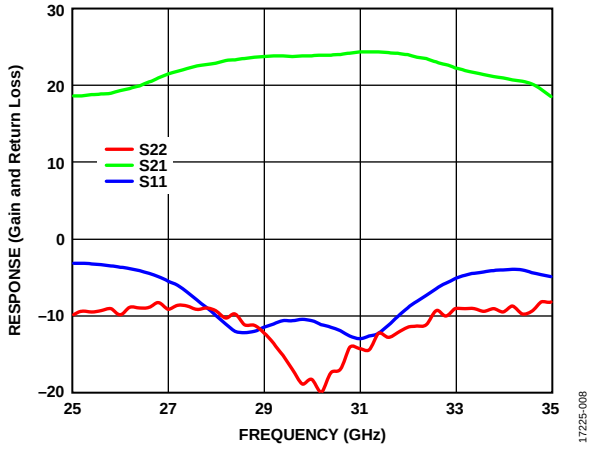


Figure 8. Response (Gain and Return Loss) vs. Frequency, V_{DDx} = 5 V, I_{DDQ} = 650 mA

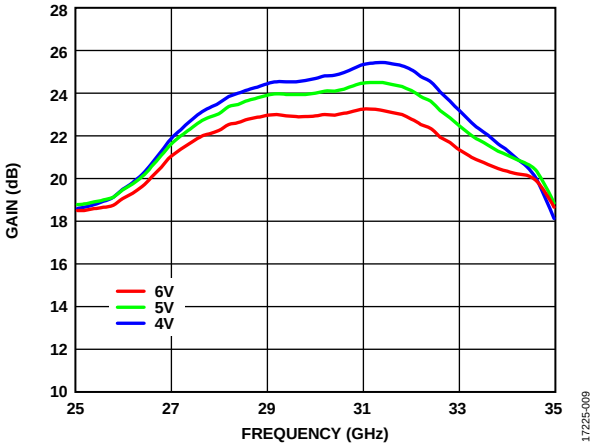


Figure 9. Gain vs. Frequency for Various Drain Bias Voltages (V_{DDx}), I_{DDQ} = 650 mA

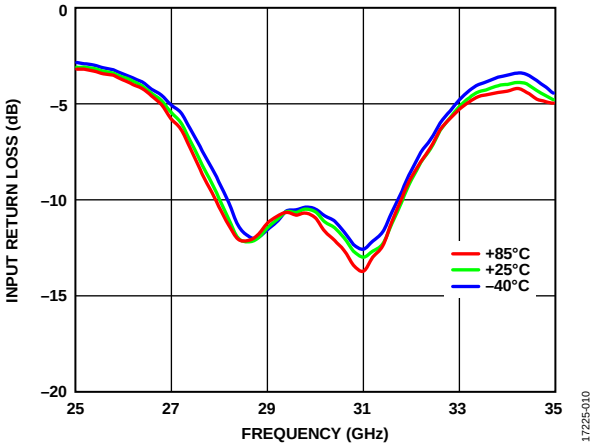


Figure 10. Input Return Loss vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

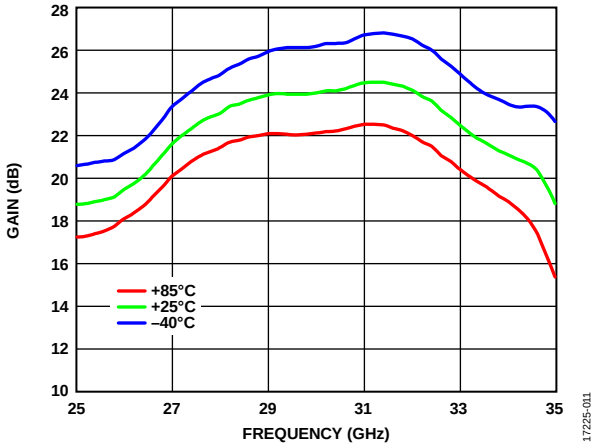


Figure 11. Gain vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

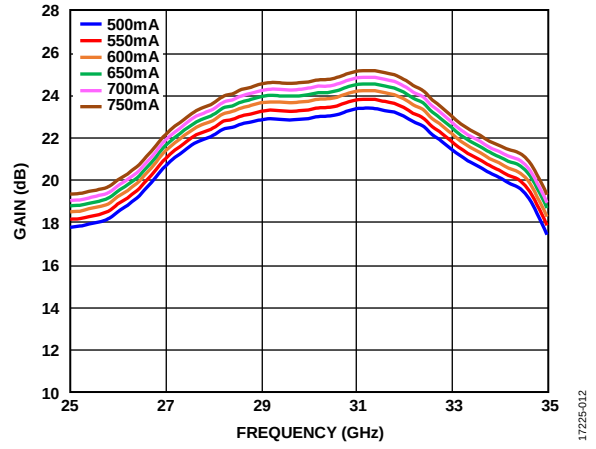


Figure 12. Gain vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V

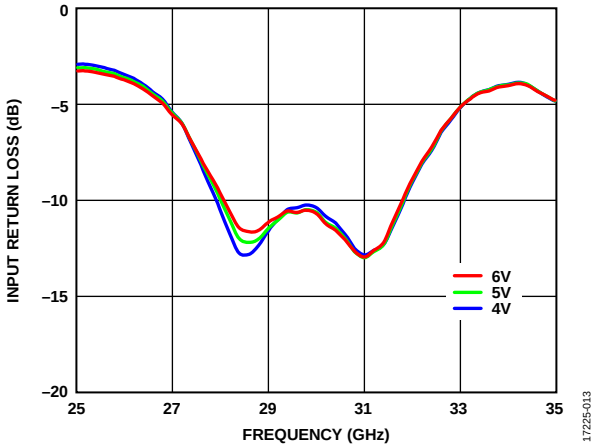


Figure 13. Input Return Loss vs. Frequency for Various Drain Bias Voltages (V_{DDx}), I_{DDQ} = 650 mA

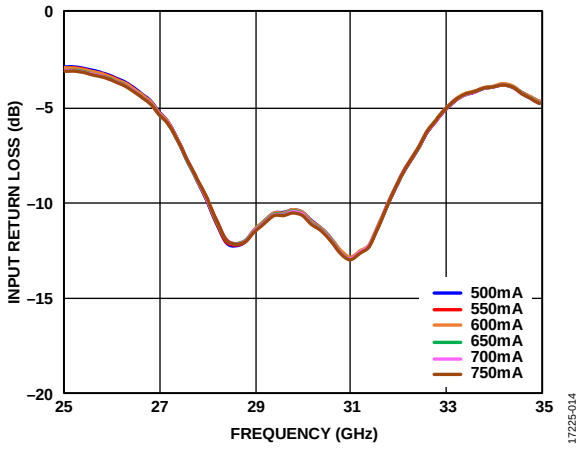


Figure 14. Input Return Loss vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V

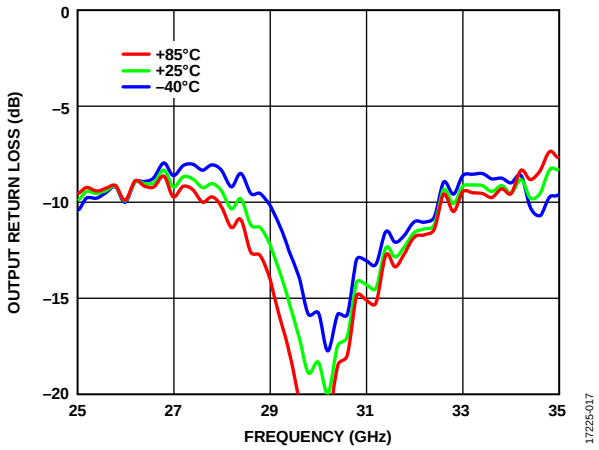


Figure 17. Output Return Loss vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

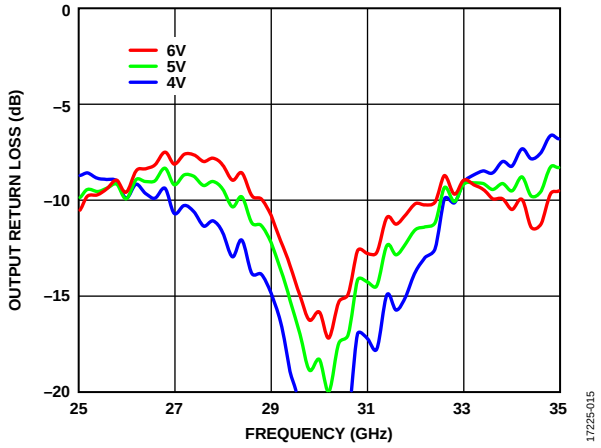


Figure 15. Output Return Loss vs. Frequency for Various Drain Bias Voltages (V_{DDx}), I_{DDQ} = 650 mA

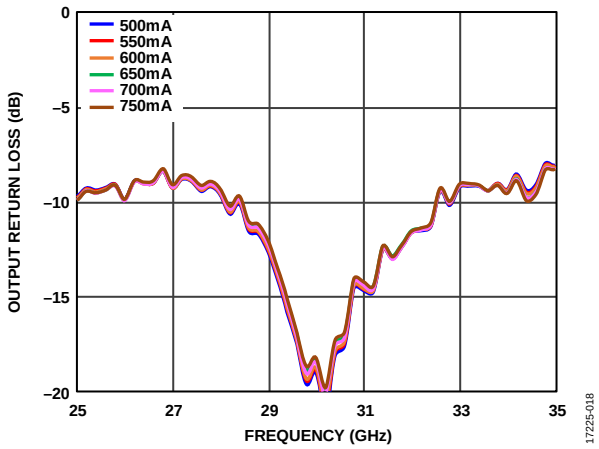


Figure 18. Output Return Loss vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V

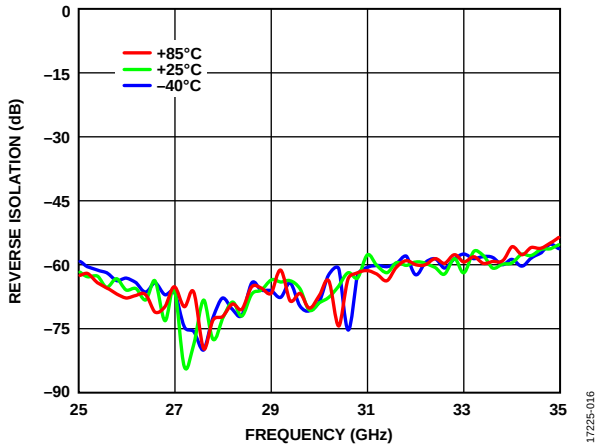


Figure 16. Reverse Isolation vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

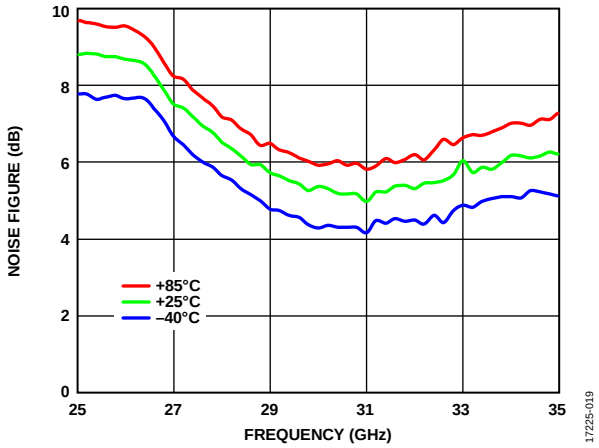


Figure 19. Noise Figure vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

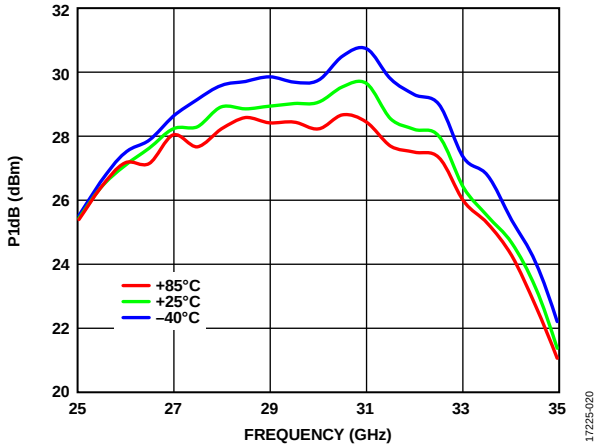


Figure 20. P1dB vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

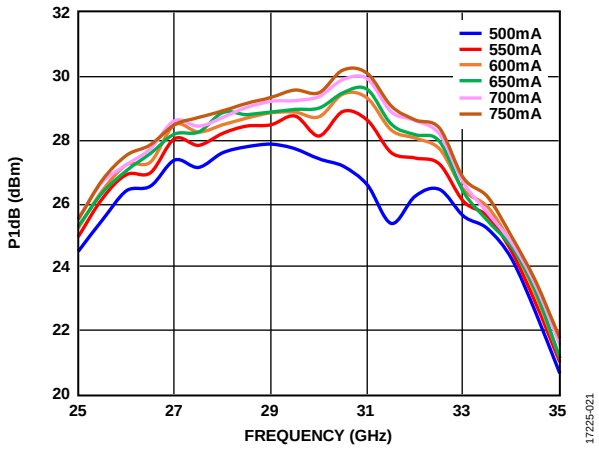


Figure 21. P1dB vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V

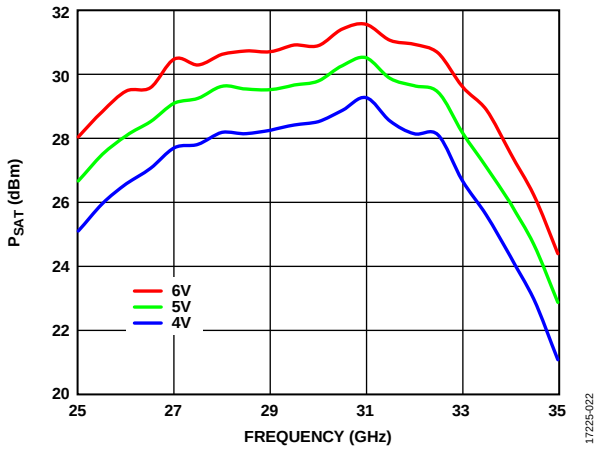


Figure 22. P_{SAT} vs. Frequency for Various Drain Bias Voltages (V_{DDx}), I_{DDQ} = 650 mA

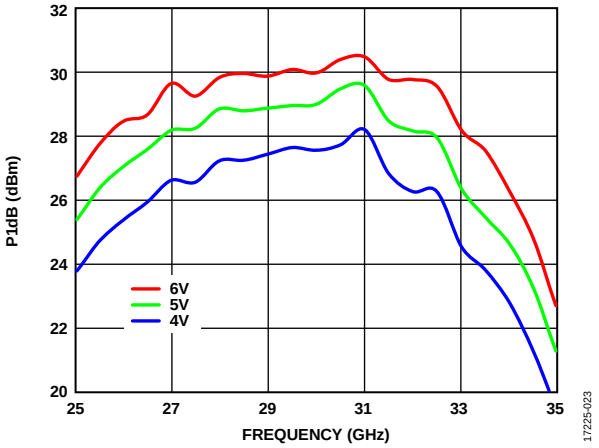


Figure 23. P1dB vs. Frequency for Various Drain Bias Voltages (V_{DDx}), I_{DDQ} = 650 mA

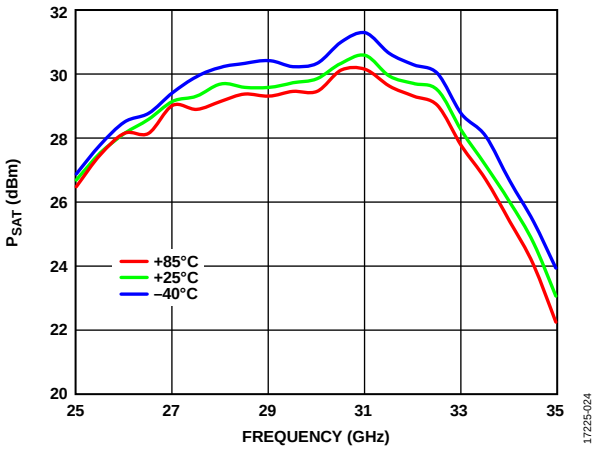


Figure 24. P_{SAT} vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA

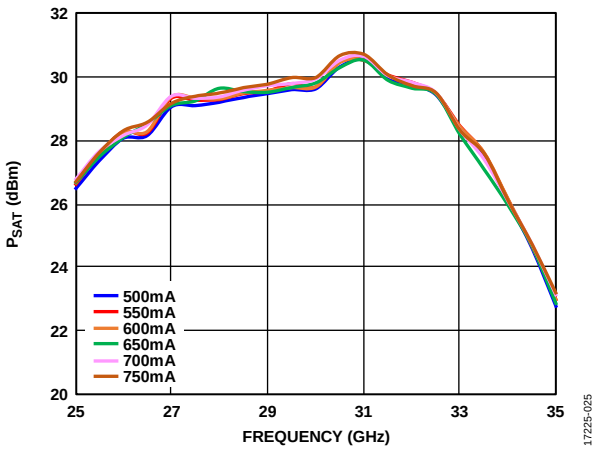


Figure 25. P_{SAT} vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V

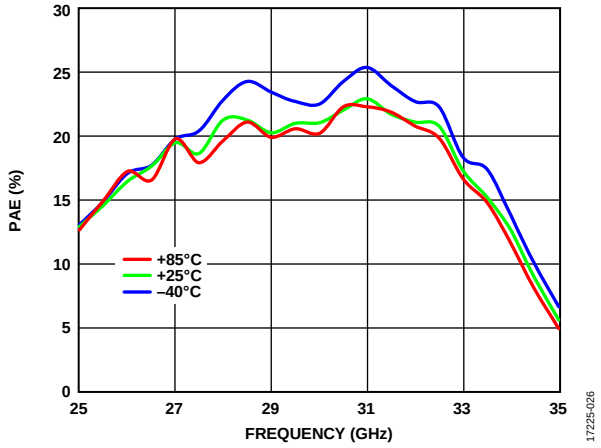


Figure 26. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, V_{DDx} = 5 V, I_{DDQ} = 650 mA, PAE Measured at P_{SAT}

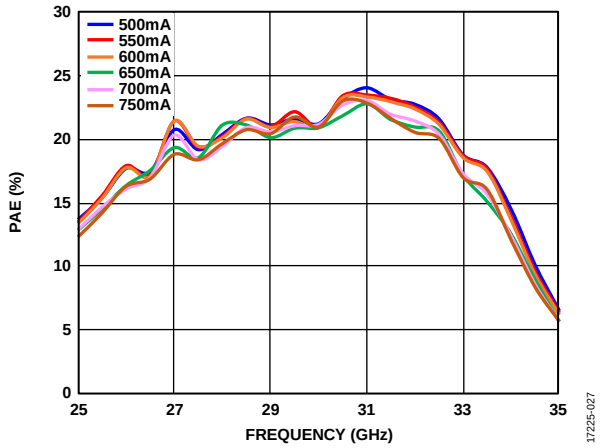


Figure 27. PAE vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V, PAE Measured at P_{SAT}

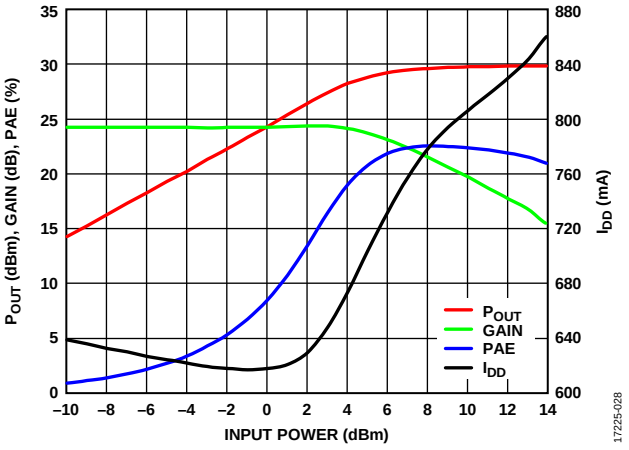


Figure 28. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), and Drain Current (I_{DD}) vs. Input Power, 29.5 GHz, V_{DDx} = 5 V, I_{DDQ} = 650 mA

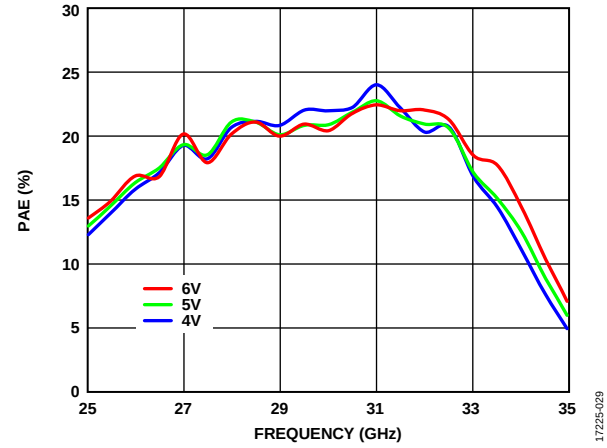


Figure 29. PAE vs. vs. Frequency for Various Drain Bias Voltages (V_{DDx}), I_{DDQ} = 650 mA, PAE Measured at P_{SAT}

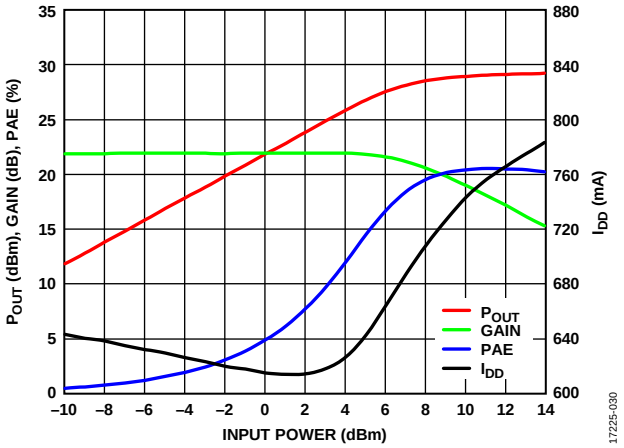


Figure 30. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), Drain Current (I_{DD}) vs. Input Power, 27 GHz, V_{DDx} = 5 V, I_{DDQ} = 650 mA

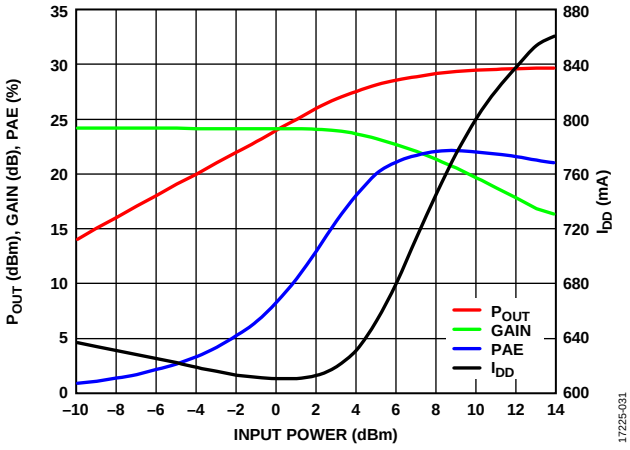


Figure 31. Output Power (P_{OUT}), Gain, Power Added Efficiency (PAE), Drain Current (I_{DD}) vs. Input Power, 32 GHz, V_{DDx} = 5 V, I_{DDQ} = 650 mA

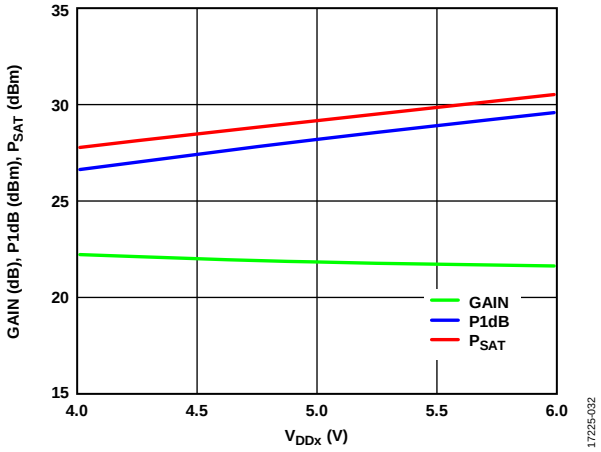


Figure 32. Gain, P1dB, and P_{SAT} vs. V_{DDx}, 27 GHz, I_{DDQ} = 650 mA

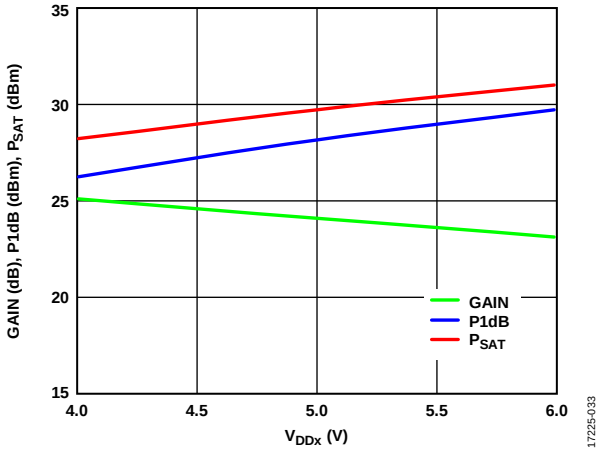


Figure 33. Gain, P1dB, and P_{SAT} vs. V_{DDx}, 32 GHz, I_{DDQ} = 650 mA

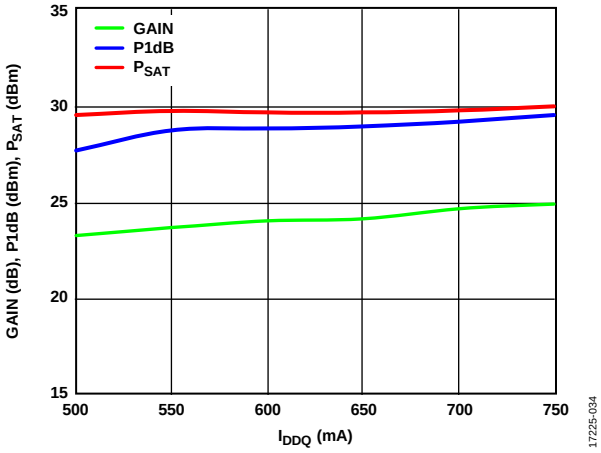


Figure 34. Gain, P1dB, and P_{SAT} vs. I_{DDQ}, 29.5 GHz, V_{DDx} = 5 V

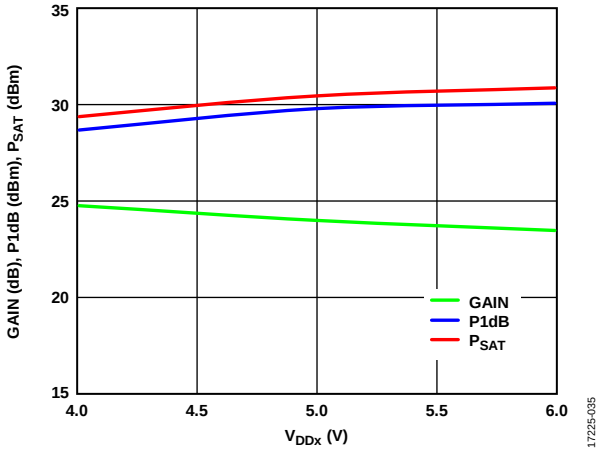


Figure 35. Gain, P1dB, and P_{SAT} vs. V_{DDx}, 29.5 GHz, I_{DDQ} = 650 mA

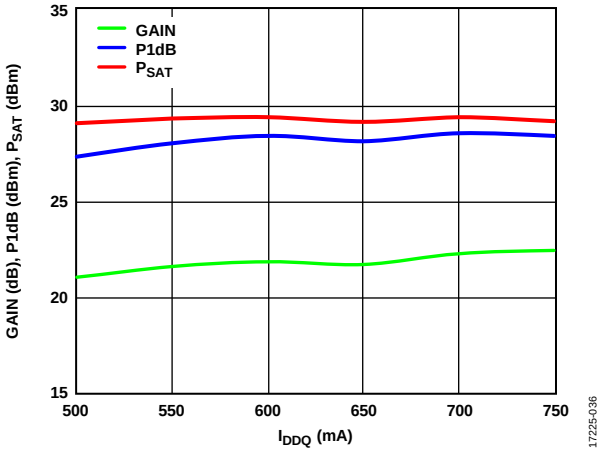


Figure 36. Gain, P1dB, and P_{SAT} vs. I_{DDQ}, 27 GHz, V_{DDx} = 5 V

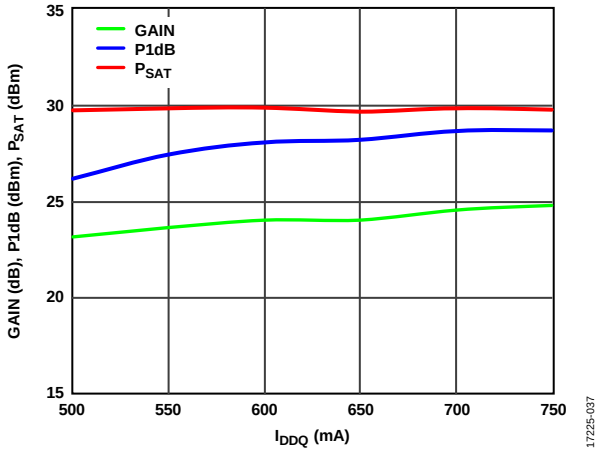


Figure 37. Gain, P1dB, and P_{SAT} vs. I_{DDQ}, 32 GHz, V_{DDx} = 5 V

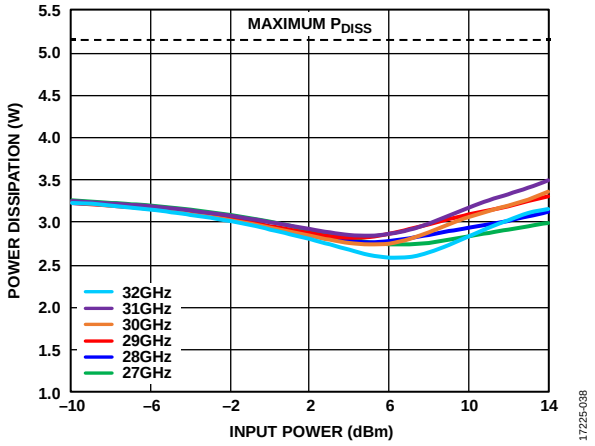


Figure 38. Power Dissipation vs. Input Power at T_A = 85°C, V_{DDx} = 5 V, I_{DDQ} = 650 mA

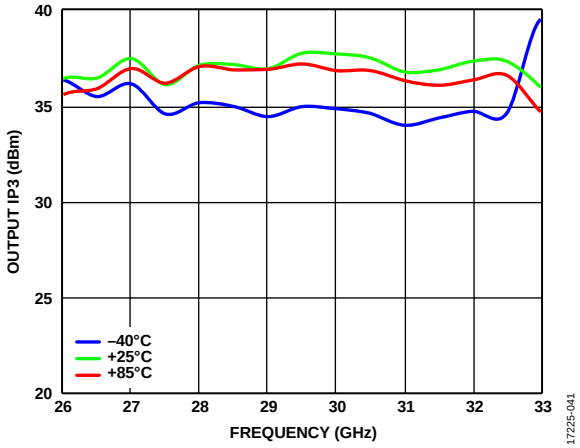


Figure 41. Output IP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 20 dBm, V_{DDx} = 5 V, I_{DDQ} = 650 mA

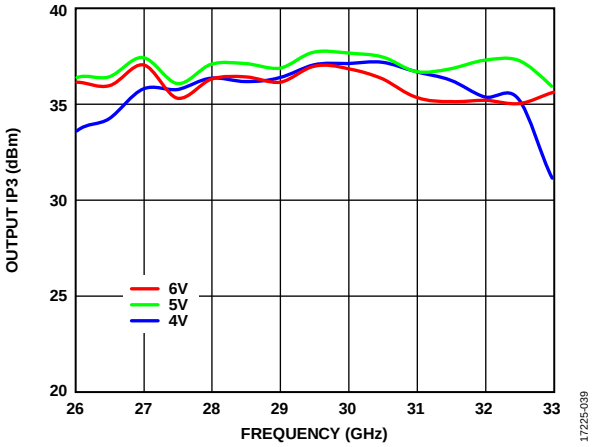


Figure 39. Output IP3 vs. Frequency for Various Supply Voltages (V_{DDx}), I_{DDQ} = 650 mA

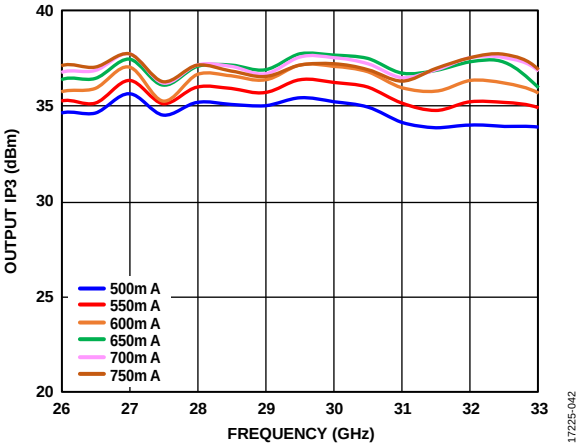


Figure 42. Output IP3 vs. Frequency for Various Quiescent Currents (I_{DDQ}), V_{DDx} = 5 V

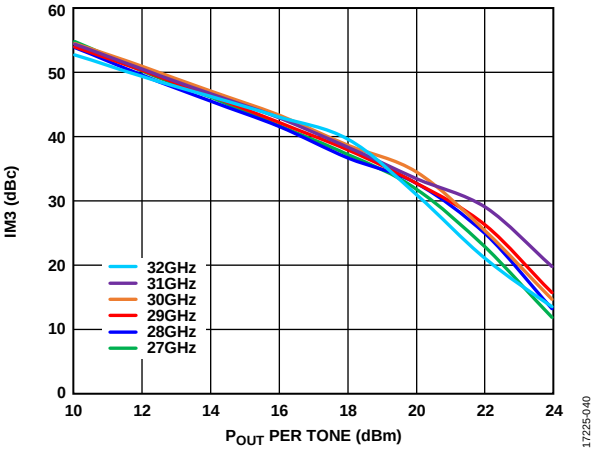


Figure 40. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT} per Tone, V_{DDx} = 4 V, I_{DDQ} = 650 mA

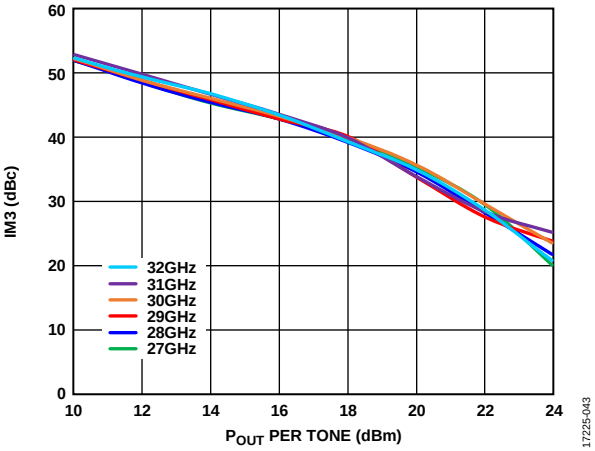


Figure 43. IM3 vs. P_{OUT} per Tone, V_{DDx} = 5 V, I_{DDQ} = 650 mA

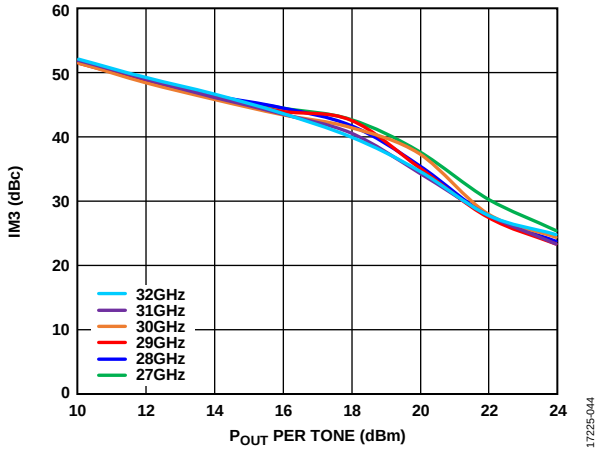


Figure 44. IM3 vs. P_{OUT} per Tone, V_{DDx} = 6 V, I_{DDQ} = 650 mA

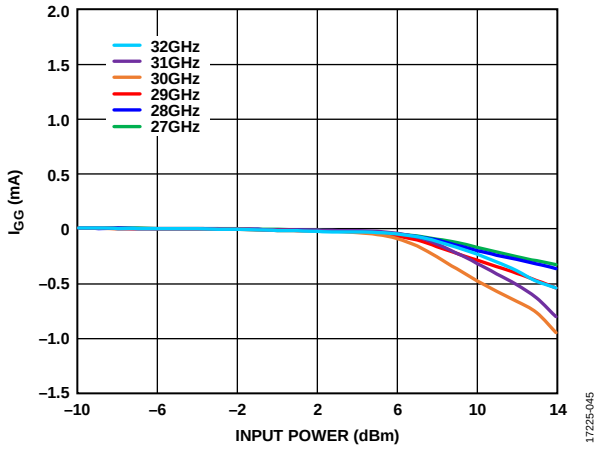


Figure 45. Gate Current (I_{GG}) vs. Input Power for Various Frequencies, V_{DDx} = 5 V, I_{DDQ} = 650 mA

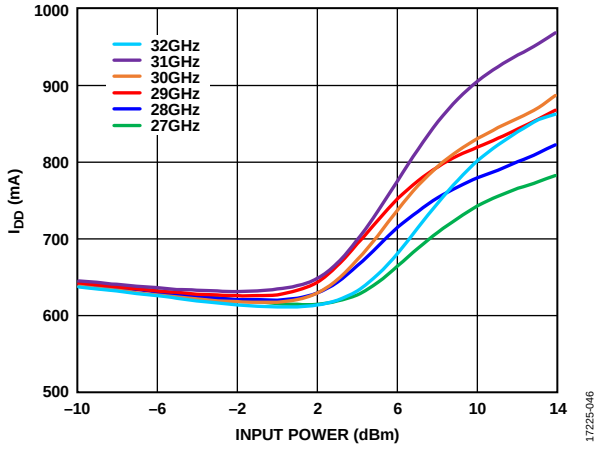


Figure 46. Drain Current (I_{DD}) vs. Input Power for Various Frequencies, V_{DDx} = 5 V, I_{DDQ} = 650 mA

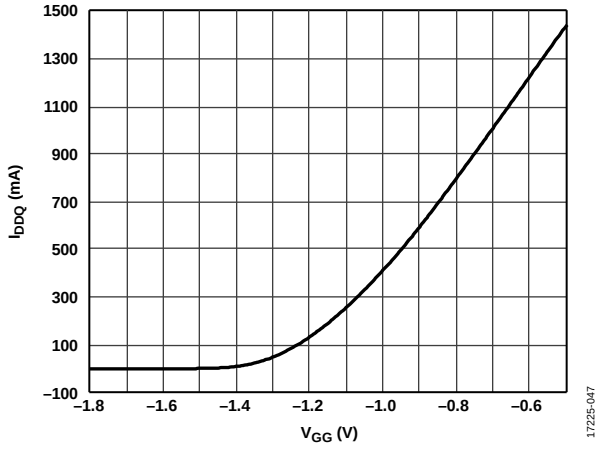


Figure 47. Quiescent Current (I_{DDQ}) vs. V_{GG}, V_{DDx} = 5 V, Representative of a Typical Device

THEORY OF OPERATION

The architecture of the HMC1132PM5E power amplifier is shown in Figure 48. The amplifier consists of a cascade of four, single-stage amplifiers. This approach provides a high P1dB as well as a high gain that is flat across the operating frequency range. V_{DD1} provides drain bias to the first three gain stages, whereas V_{DD2} provides drain bias to the fourth gain stage. V_{GG} provides gate bias to all four gain stages, allowing control of the quiescent current. RFIN and RFOUT provide dc paths to GND as a way of increasing the overall ESD robustness of the device.

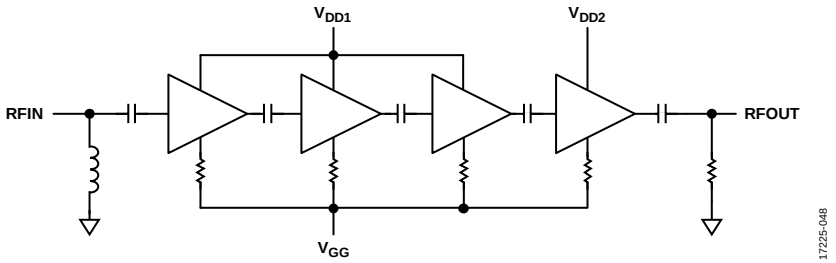


Figure 48. Architecture and Simplified Block Diagram

APPLICATIONS INFORMATION

The HMC1132PM5E is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for V_{DD1}, V_{DD2}, and V_{GG} (see Figure 49). The drain bias voltage must be applied to both V_{DD1} and V_{DD2}, and the gate bias voltage must be applied to V_{GG}. Although the RFIN and RFOUT ports ac couple the signal, dc paths to GND are provided to increase the ESD robustness of the device. External dc blocking of RFIN and/or RFOUT is desirable when appreciable levels of dc are present.

All measurements for this device were taken using the typical application circuit shown in Figure 49, configured as shown on the evaluation PCB (see Figure 50).

The following bias sequence is recommended during power-up:

1. Connect the evaluation board to ground.
2. Set the gate bias voltage to −2 V.
3. Set the drain bias voltages to 5 V.
4. Increase the gate bias voltage to achieve a quiescent I_{DDQ} = 650 mA.
5. Apply the RF signal.

The following bias sequence is recommended during power-down:

1. Turn off the RF signal.
2. Decrease the gate bias voltage to −2 V to achieve an I_{DDQ} = 0 mA (approximately).
3. Decrease the drain bias voltages to 0 V.
4. Increase the gate bias voltage to 0 V.

The V_{DDx} = 5 V and I_{DDQ} = 650 mA bias conditions are the operating points recommended to optimize the overall performance of the device. Unless otherwise noted, the data shown was obtained using the recommended bias conditions. Operation of the HMC1132PM5E at different bias conditions may provide performance that differs from what is shown in the Typical Performance Characteristics section. Biasing the HMC1132PM5E for a higher drain current typically results in higher P1dB, P_{SAT}, and gain, though at the expense of increased power consumption.

APPLICATION CIRCUIT

Figure 49 shows the typical application circuit.

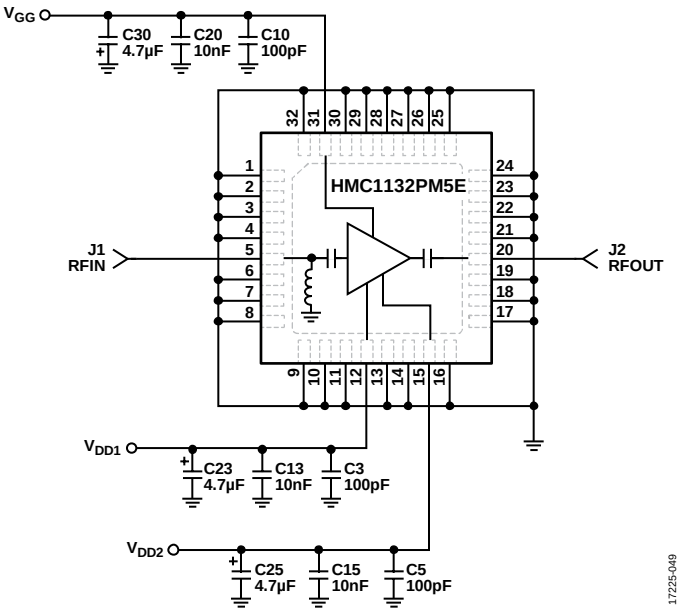


Figure 49. Typical Application Circuit

EVALUATION BOARD

The HMC1132PM5E evaluation board is a 2-layer board fabricated using Rogers 4350 and best practices suited for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance. The circuit board is attached to a heat sink. Components are mounted using SN63 solder, allowing rework of the surface-mount components without compromising attachment of the PCB to a heat sink.

The evaluation board and populated components are designed to operate over the ambient temperature range of −40°C to +85°C.

During operation, to control the temperature of the HMC1132PM5E, attach the evaluation board to a temperature controlled plate. For the proper bias sequence, see the Applications Information section.

The evaluation board schematic is shown in Figure 51. A fully populated and tested evaluation board (see Figure 50) is available from Analog Devices, Inc., upon request.

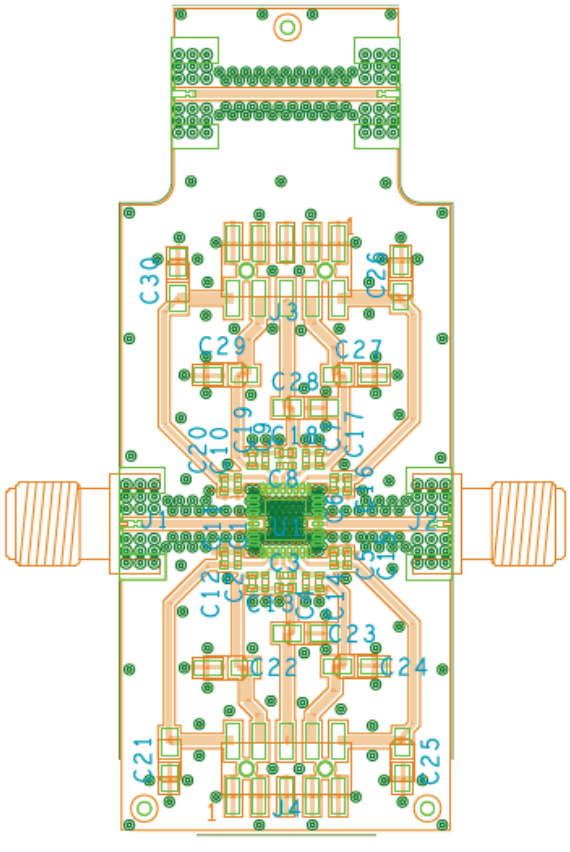


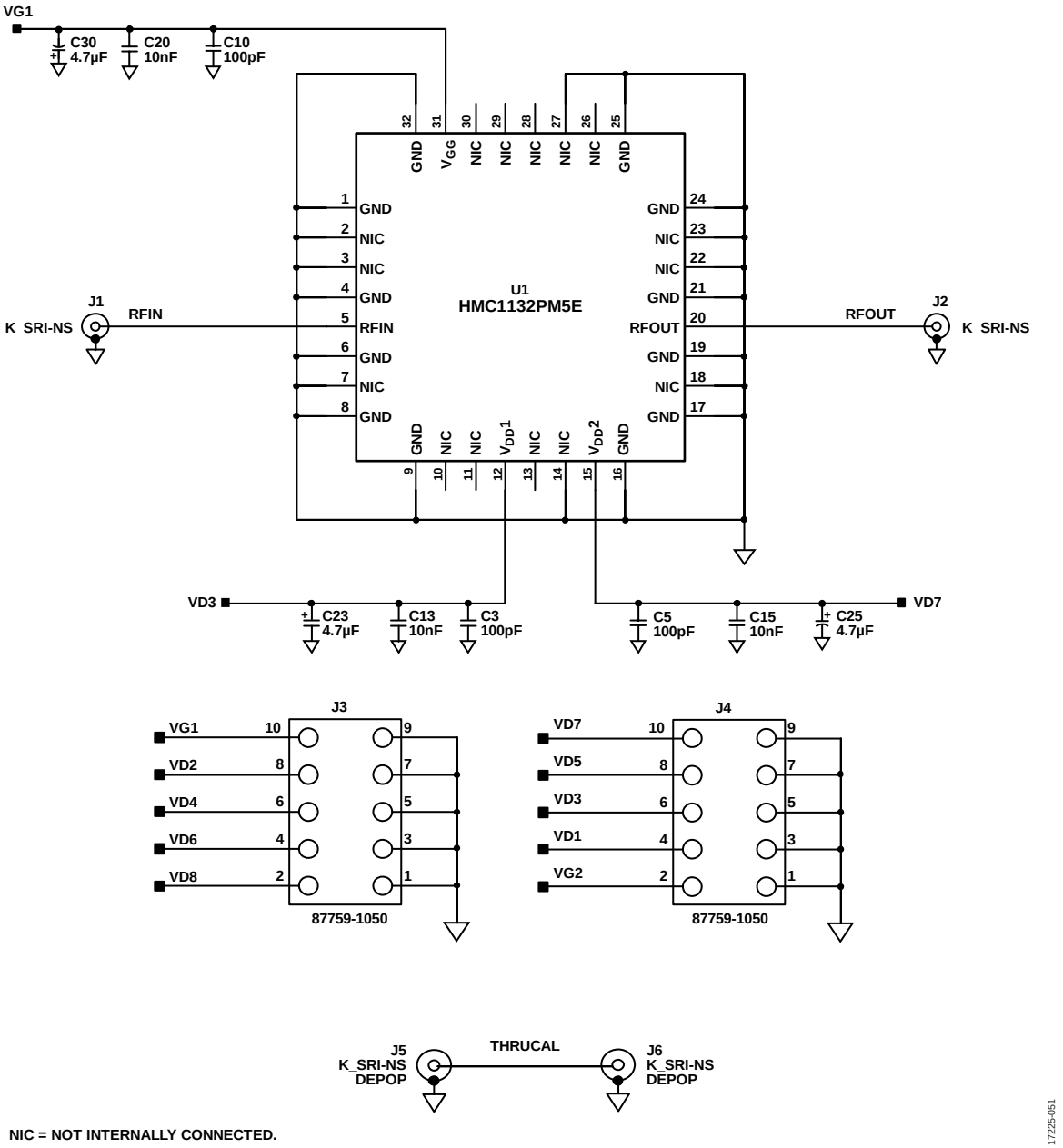
Figure 50. Evaluation PCB

BILL OF MATERIALS

Table 6. Bill of Materials for Evaluation PCB EV1HMC1132PM5

Item	Description
J1, J2	Connector, SRI K connector. SRI Part Number 25-146-1000-92.
J3, J4	DC pins.
J5, J6	Connector, SRI K connector. Not populated.
C3, C5, C10	100 pF capacitors, 0402 package.
C13, C15, C20	10 nF capacitors, 0402 package.
C23, C25, C30	4.7 µF capacitors, Case A package.
U1	HMC1132PM5E amplifier.
Heat Sink	Used for thermal transfer from the HMC1132PM5E amplifier.
PCB	08_047754 evaluation board. Circuit board material: Rogers 4350.

EVALUATION BOARD SCHEMATIC



NIC = NOT INTERNALLY CONNECTED.

Figure 51. Evaluation Board Schematic

OUTLINE DIMENSIONS

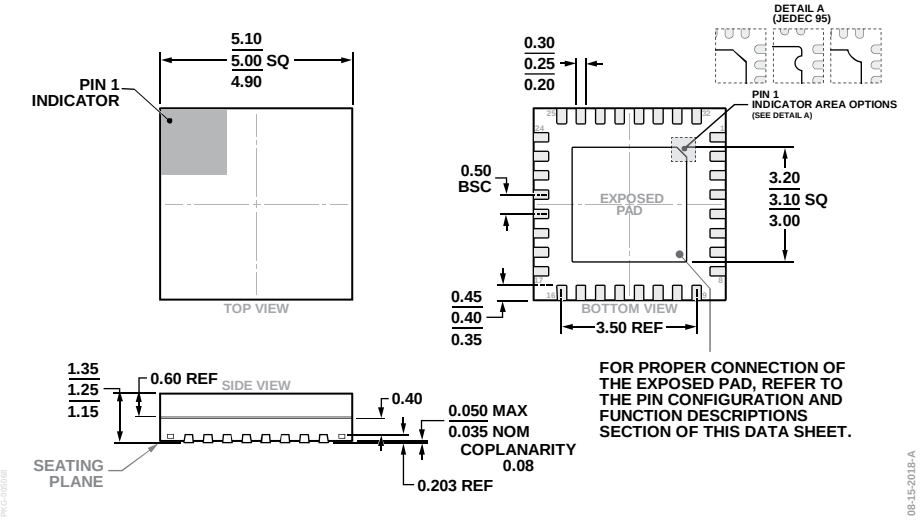


Figure 52. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature	MSL Rating[3]	Description[4]	Package Option
HMC1132PM5E	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
HMC1132PM5ETR	−40°C to +85°C	MSL3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
EV1HMC1132PM5			Evaluation Board	

[1] All models are RoHS compliant parts.
[2] When ordering the evaluation board only, reference the model number, EV1HMC1132PM5.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC1132PM5E and the HMC1132PM5ETR is nickel palladium gold (NiPdAu).