Keywords: interleaved bus operation, IBO, framers, MUX, PCI, frame interleaving, hdlc controller, T1, E1, T3, E3

APPLICATION NOTE 3760

Interleaved Bus Operation

Mar 20, 2006

Abstract: This application note shows how to configure the Interleaved Bus Operation (IBO) with the DS21FF44 framers by using the DS31256 HDLC controller onto a PCI bus. Other Dallas Semiconductor framers and transceivers will be used as well.

Overview

This application note describes how to configure an E1 framer for Interleaved Bus Operation (IBO). Interleaved Bus Operation (IBO) is designed for multiplexing data streams from numerous devices onto a single bus. The DS21FF44 framers will be used with a DS31256 HDLC controller onto a PCI bus (**Figure 1**). Other Maxim/Dallas Semiconductor T1/E1 framers and transceivers will also be featured. The hardware connections will be identical on a T1 framer.

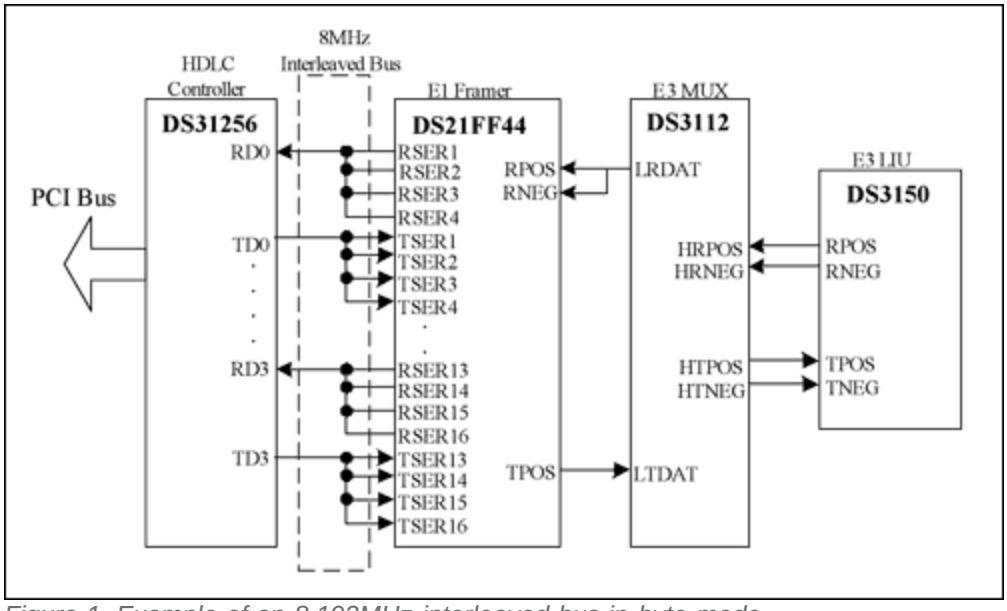

Figure 1. Example of an 8.192MHz interleaved bus in byte mode.

Hardware

Figure 2 illustrates a normal configuration of hardware connections. If the application requires frame interleaving, then TCLK and RCLK must be frequency-locked to TSYSCLK and RSYSCLK (i.e., frame

slips cannot occur). Frame slips are acceptable in byte-interleaved applications. Also, RSYNC and TSSYNC must be tied together. (In IBO mode the receiver is not independent of the transmitter.)

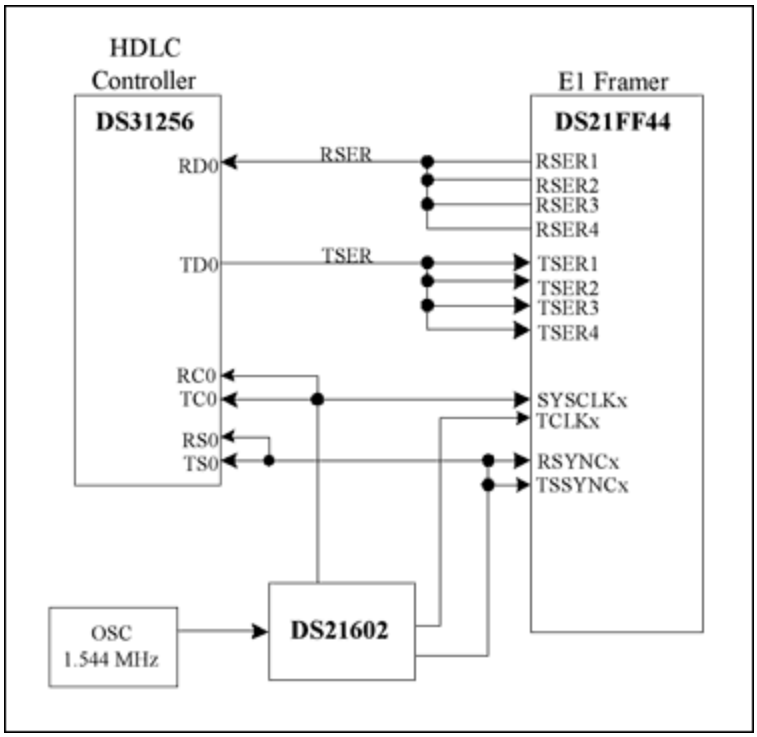

Figure 2. Connections for IBO mode.

The sync pulse must be phase-locked to the 8.192MHz clock, as shown in **Figure 3**. The hardware for a T1 framer differs only in the use of a 1.544MHz clock to connect to TCLK/RCLK instead of an E1 frequency clock. Furthermore, in T1 every fourth channel is unused and forced to 0xFF. Consult the IBO section in the T1 data sheet for details.

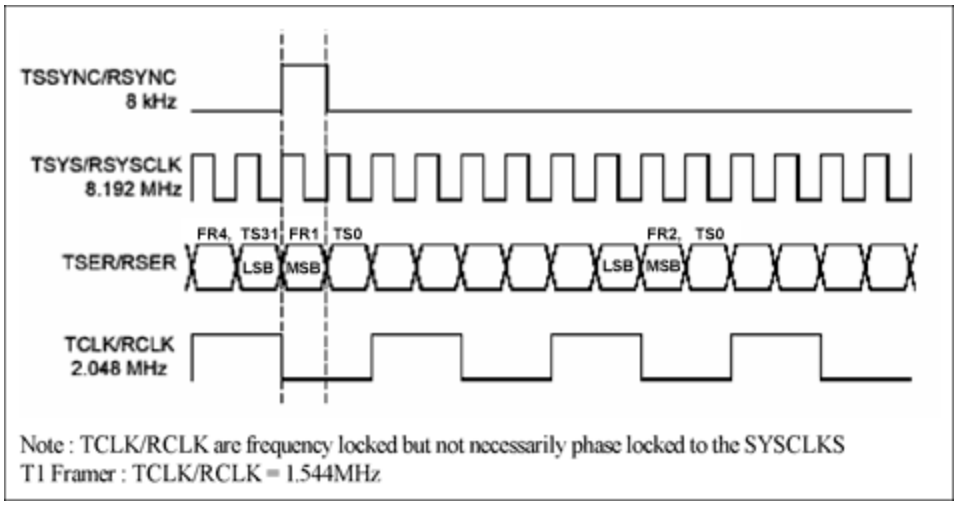

Figure 3. Timing diagrams for IBO mode.

Refer to Section 22 of the DS21FF44 data sheet for additional timing diagrams. More information about the IBO can be found in Section 20 of the data sheet.

Software

The chip must be configured for IBO functionality. Configuration includes the setting the IBO registers, enabling the elastic stores, and configuring TSYNC and RSYNC correctly. (See the detailed register listing in the **Table 1** below.) Additionally, users must select the 2.048MHz mode for the system clocks (for both T1 and E1 framers).

Table 1. The Bits That Must Be Set on All 16 Framers

DS21FF42/FT42 DS21Q44 DS21354/554 Registers	DS21352/552 DS21Q42 Registers	Comment
RCR1.5 = 1	RCR2.3 = 1	RSYNC is an input.
RCR2.1 = 1	CCR1.2 = 1	Receive elastic store is enabled.
RCR2.2 = 1	CCR1.3 = 1	RSYSCLK is 2.048/4.096/8.192 MHz.
TCR1.0 = 1	TCR2.2 = 1	TSYNC is an output.
CCR3.1 = 1	CCR1.4 = 1	TSYSCLK is 2.048/4.096/8.192 MHz.
CCR3.7 = 1	CCR1.7 = 1	Transmit elastic store is enabled.
IBO = 0x09	IBO = 0x09	IBO enabled, byte mode, master devices (framers 1, 5, 9, 13)
IBO = 0x08	IBO = 0x08	IBO enabled, byte mode, slave devices (framers 2-4, 6-8, 10-12, 14-16)

Conclusion

This application note has shown how to configure a DS21FF44 for Interleaved Bus Operation (IBO) with various Dallas Semiconductor HDLC controller, E1 framer, and transceiver devices.

If you have further questions about our framers, transceivers or HDLC controller products, please contact the Telecommunication Applications support team.

Related Parts		
DS21352	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21354	3.3V/5V E1 Single Chip Transceivers (SCT)	
DS21552	3.3V DS21352 and 5V DS21552 T1 Single Chip Transceivers	
DS21554	3.3V/5V E1 Single Chip Transceivers (SCT)	Free Samples
DS21602	3.3V/5V Clock Rate Adapter	Free Samples
DS21FF42	4 x 4 16 Channel T1 Framer / 4 x 3 12 Channel T1 Framer	
DS21FF44	4x3 Twelve Channel E1 Framer / 4x4 Sixteen Channel E1 Framer	

DS21FT42	4 x 4 16 Channel T1 Framer / 4 x 3 12 Channel T1 Framer	
DS21FT44	4x3 Twelve Channel E1 Framer / 4x4 Sixteen Channel E1 Framer	Free Samples
DS21Q352	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q354	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q42	Enhanced Quad T1 Framer	
DS21Q44	Enhanced Quad E1 Framer	
DS21Q552	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS21Q554	Quad T1/E1 Transceiver (3.3V, 5.0V)	
DS3112	TEMPE T3 E3 Multiplexer, 3.3V T3/E3 Framer and M13/E13/G.747 MUX	Free Samples
DS31256	256-Channel, High-Throughput HDLC Controller	

More Information
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