74LVC2G125

Dual bus buffer/line driver; 3-state

Rev. 16 — 10 September 2018 Product data sheet

1. General description

The 74LVC2G125 provides a dual non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (pin n$\overline{OE}$). A HIGH-level at pin n$\overline{OE}$ causes the output to assume a high-impedance OFF-state. Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
- • JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
- • HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low-power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC2G125DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC2G125DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC2G125GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74LVC2G125GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74LVC2G125GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2
74LVC2G125GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74LVC2G125GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code [1]
74LVC2G125DP	V25
74LVC2G125DC	V25
74LVC2G125GT	V25
74LVC2G125GF	VM
74LVC2G125GM	V25
74LVC2G125GN	VM
74LVC2G125GS	VM

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

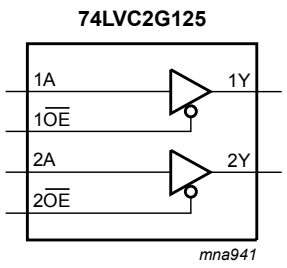


Fig. 1. Logic symbol

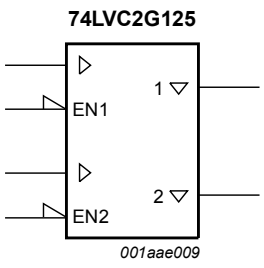


Fig. 2. IEC logic symbol

6. Pinning information

6.1. Pinning

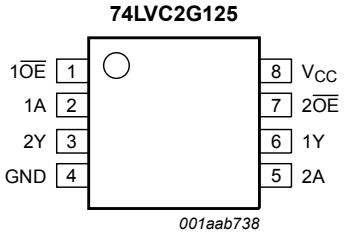


Fig. 3. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

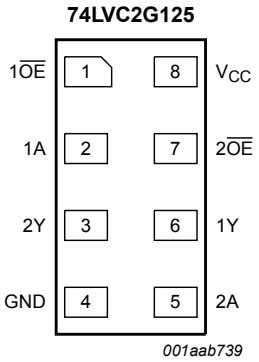


Fig. 4. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203 (XSON8)

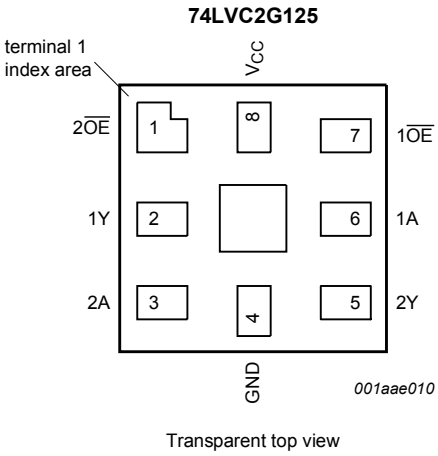


Fig. 5. Pin configuration SOT902-2 (XQFN8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT1116 and SOT1203	SOT902-2	
$1\overline{OE}$, $2\overline{OE}$	1, 7	7, 1	output enable input (active LOW)
1A, 2A	2, 5	6, 3	data input
GND	4	4	ground (0 V)
1Y, 2Y	6, 3	2, 5	data output
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
$n\overline{OE}$	**nA**	**nY**
L	L	L
L	H	H
H	X	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Enable mode	[1]	-0.5	V_{CC} + 0.5	V
		Disable mode	[1]	-0.5	+6.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For VSSOP8 package: above 110 °C the value of P_{tot} derates linearly with 8 mW/K.
For XSON8, XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	V_{CC} = 1.65 V to 5.5 V; Enable mode	0	V_{CC}	V
		V_{CC} = 1.65 V to 5.5 V; Disable mode	0	5.5	V
		V_{CC} = 0 V; Power-down mode	0	5.5	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}	-	-	0.65V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}	-	-	0.7V_{CC}	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35V_{CC}	-	0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3V_{CC}	-	0.3V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.3	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	-	0.80	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V_{CC} - 0.1	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	-	-	3.4	-	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	-	±0.1	±2	-	±2	µA
I_{OFF}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	±0.1	±2	-	±2	µA
I_{CC}	supply current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_O = 0 A	-	0.1	4	-	4	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	5	500	-	500	µA
C_I	input capacitance		-	2	-	-	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.

11. Dynamic characteristics

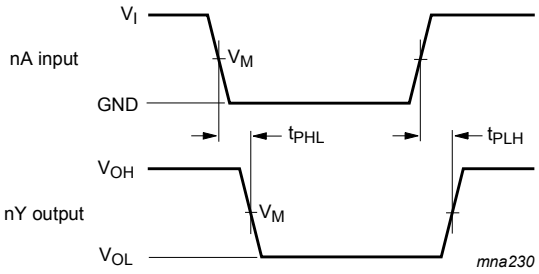
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground 0 V); for test circuit see Fig. 8.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Fig. 6 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.7	9.1	1.0	11.4	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.5	4.8	0.5	6.0	ns
		V_{CC} = 2.7 V	1.0	2.7	4.8	1.0	6.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.3	4.3	0.5	5.5	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.9	3.7	0.5	4.6	ns
t_{en}	enable time	$n\overline{OE}$ to nY; see Fig. 7 [3]						
		V_{CC} = 1.65 V to 1.95 V	1.5	4.3	9.9	1.5	12.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.8	5.6	1.0	7.0	ns
		V_{CC} = 2.7 V	1.5	3.3	5.7	1.5	7.1	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.4	4.7	0.5	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	2.0	3.8	0.5	4.8	ns
t_{dis}	disable time	$n\overline{OE}$ to nY; see Fig. 7 [4]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.5	11.6	1.0	14.1	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	1.8	5.8	0.5	7.6	ns
		V_{CC} = 2.7 V	1.0	2.7	4.8	1.0	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.7	4.6	1.0	5.9	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.8	3.4	0.5	4.6	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [5]						
		output enabled	-	18	-	-	-	pF
		output disabled	-	5	-	-	-	pF

[1] Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{en} is the same as t_{PZH} and t_{PZL}.
[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

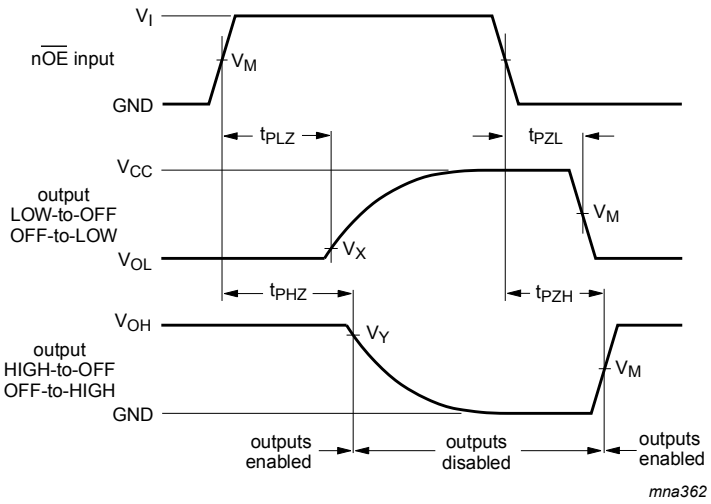
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Propagation delay input (nA) to output (nY)



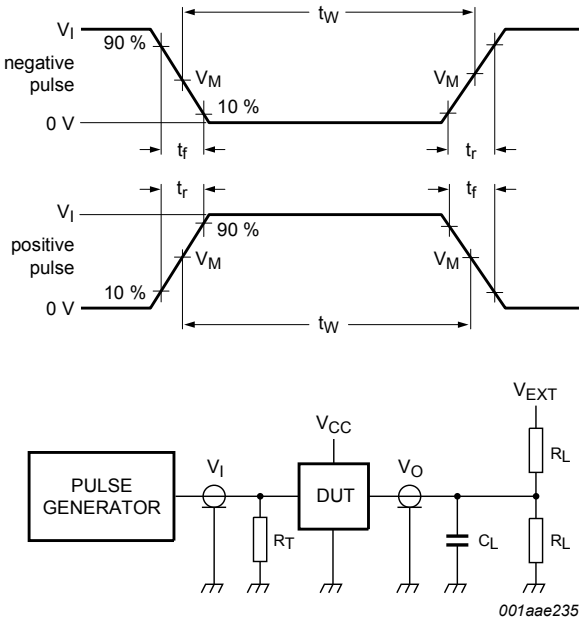
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state output enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

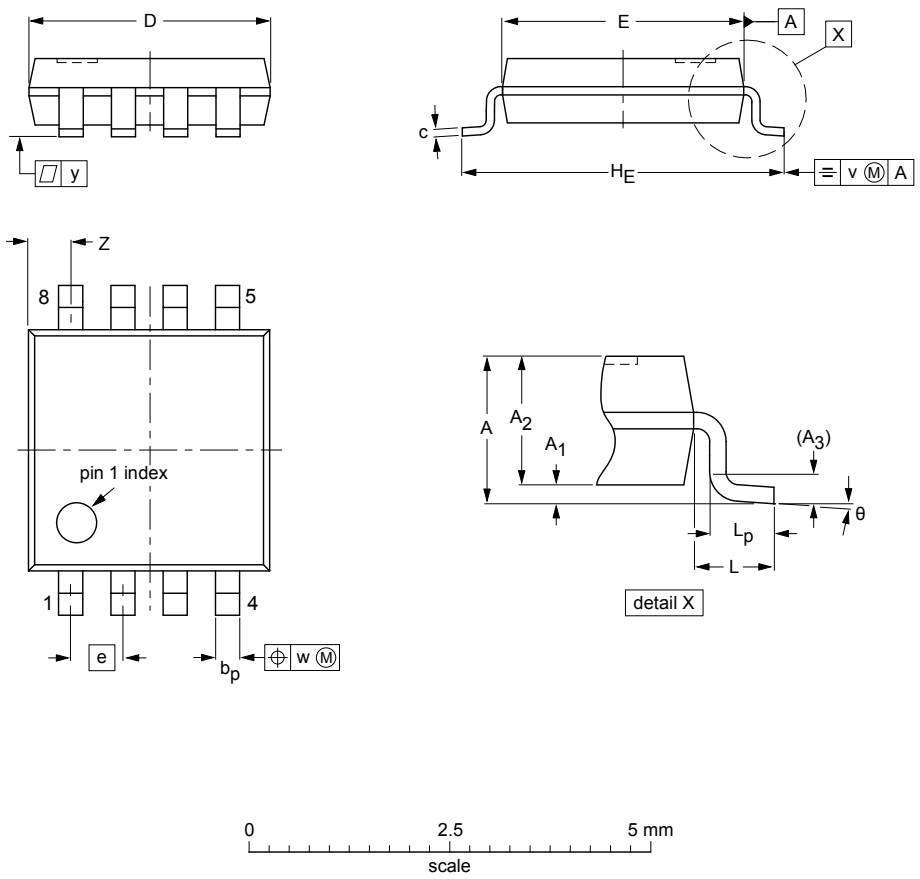
Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

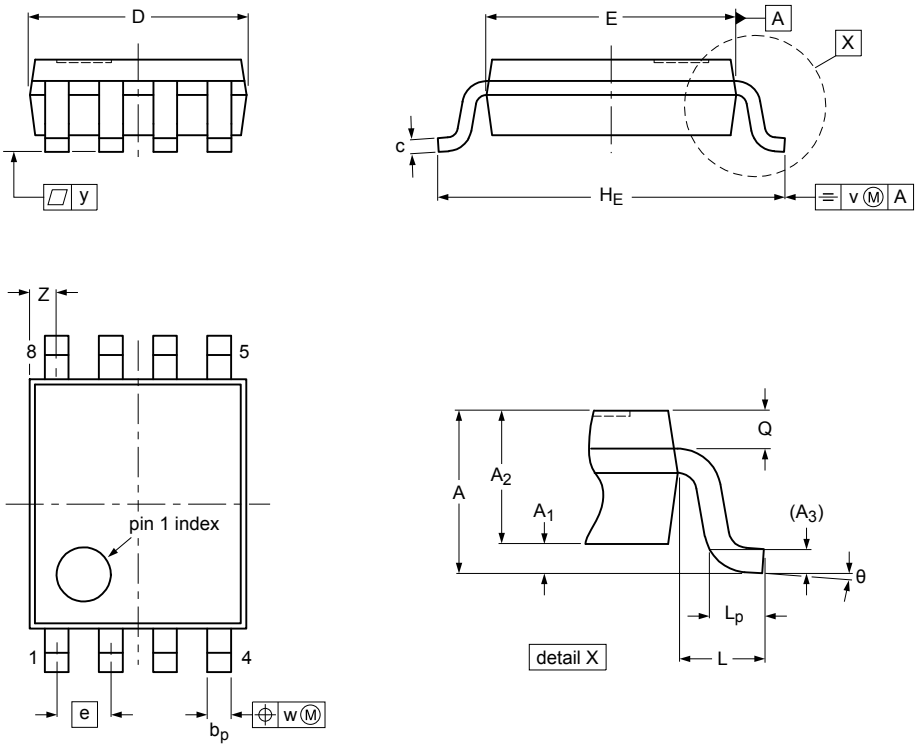
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 9. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm max	1	0.15	0.85	0.12	0.27	0.23	2.1	2.4	0.5	3.2	0.4	0.40	0.21	0.2	0.08	0.1	0.4	8°
nom																		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

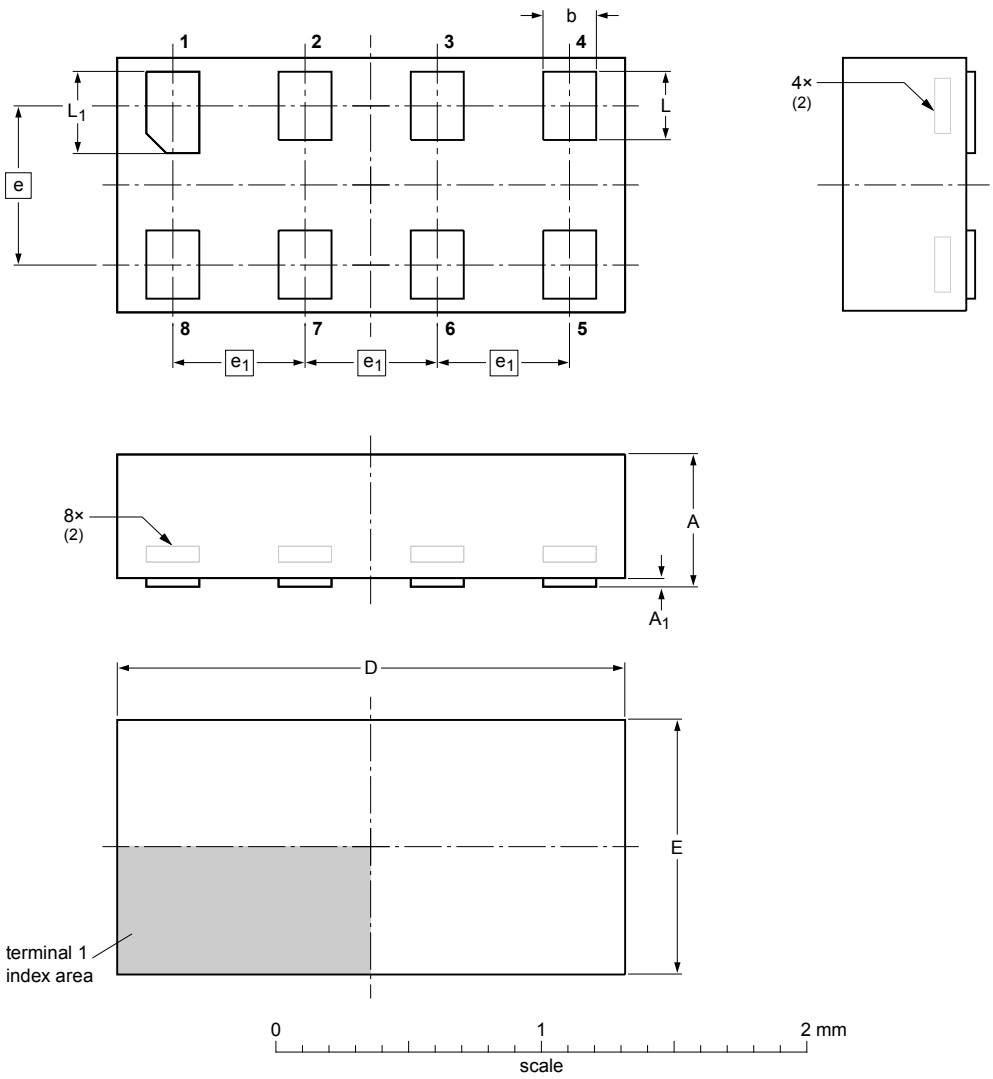
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

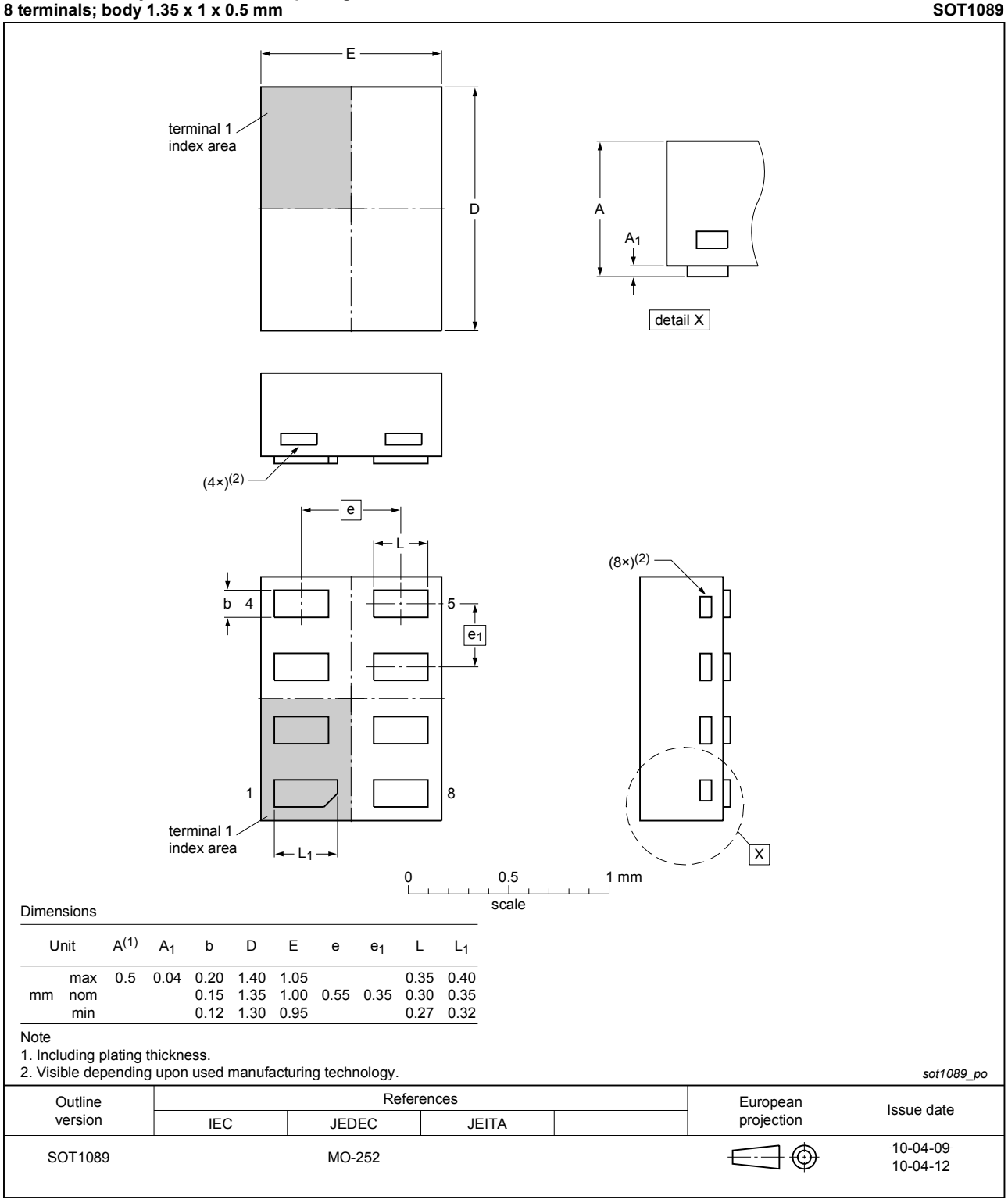
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig. 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

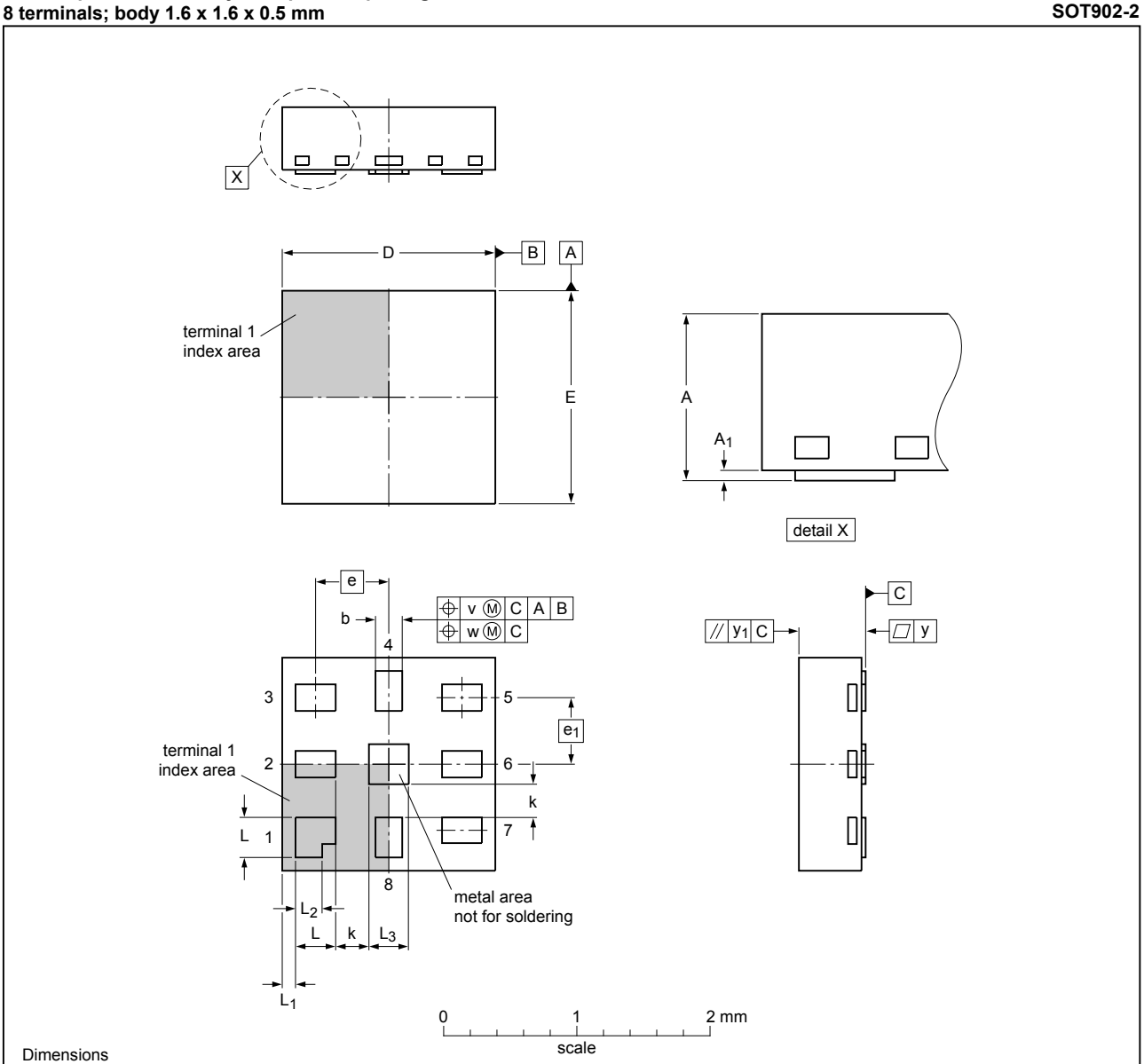
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Fig. 12. Package outline SOT1089 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit[1]		A	A_1	b	D	E	e	e_1	k	L	L_1	L_2	L_3	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65				0.35	0.15	0.25	0.35				
	nom			0.20	1.60	1.60	0.55	0.5		0.30	0.10	0.20	0.30	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.2	0.25	0.05	0.15	0.25				

Note

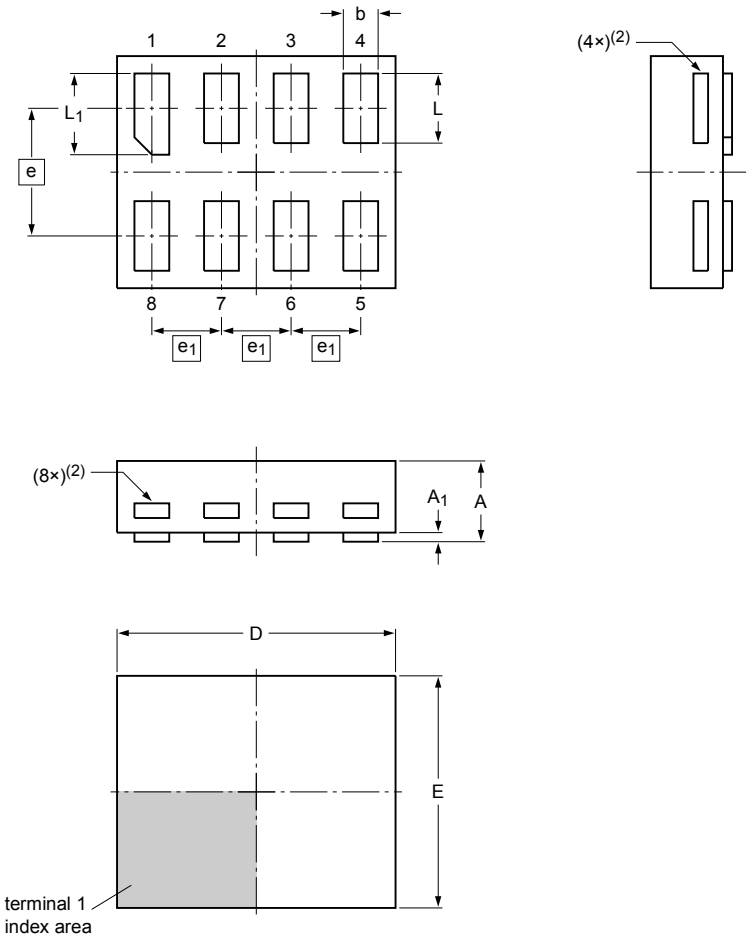
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~16-07-14~~ 16-11-08

Fig. 13. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm **SOT1116**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

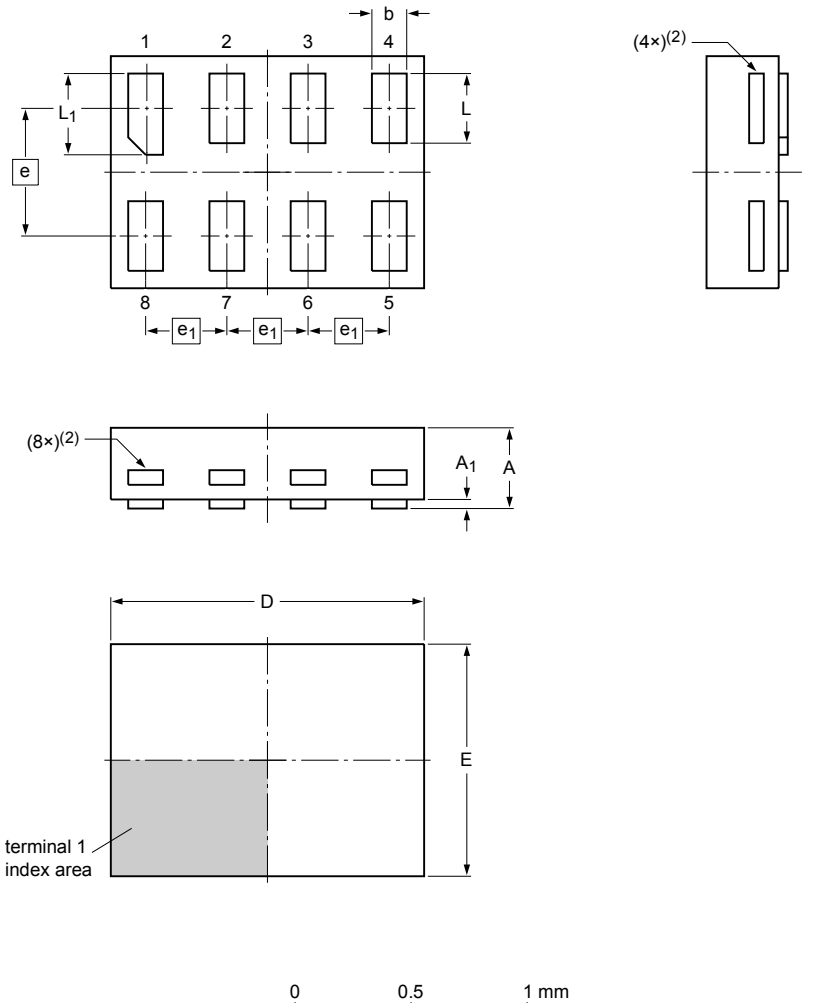
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07

Fig. 14. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm **SOT1203**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig. 15. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G125 v.16	20180910	Product data sheet	-	74LVC2G125 v.15
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74LVC2G125GD and (SOT996-2) removed.			
74LVC2G125 v.15	20161215	Product data sheet	-	74LVC2G125 v.14
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC2G125 v.14	20130329	Product data sheet	-	74LVC2G125 v.13
Modifications:	• For type number 74LVC2G125GD XSON8U has changed to XSON8.			
74LVC2G125 v.13	20120622	Product data sheet	-	74LVC2G125 v.12
Modifications:	• For type number 74LVC2G125GM the SOT code has changed to SOT902-2.			
74LVC2G125 v.12	20111201	Product data sheet	-	74LVC2G125 v.11
Modifications:	• Legal pages updated.			
74LVC2G125 v.11	20100909	Product data sheet	-	74LVC2G125 v.10
74LVC2G125 v.10	20080611	Product data sheet	-	74LVC2G125 v.9
74LVC2G125 v.9	20080226	Product data sheet	-	74LVC2G125 v.8
74LVC2G125 v.8	20070907	Product data sheet	-	74LVC2G125 v.7
74LVC2G125 v.7	20060523	Product data sheet	-	74LVC2G125 v.6
74LVC2G125 v.6	20051223	Product data sheet	-	74LVC2G125 v.5
74LVC2G125 v.5	20050201	Product specification	-	74LVC2G125 v.4
74LVC2G125 v.4	20040922	Product specification	-	74LVC2G125 v.3
74LVC2G125 v.3	20040109	Product specification	-	74LVC2G125 v.2
74LVC2G125 v.2	20030901	Product specification	-	74LVC2G125 v.1
74LVC2G125 v.1	20030310	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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