

## TPS7B4250-Q1 50-mA 40-V Voltage-Tracking LDO With 5-mV Tracking Tolerance

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- $-20\text{-V}$  to  $45\text{-V}$  Wide, Maximum Input Voltage Range
- Output Current, 50 mA
- Very-Low Output-Tracking Tolerance, 5 mV (max)
- 150-mV Low Dropout Voltage When  $I_{\text{OUT}} = 10\text{ mA}$
- Combined Reference and Enable Input
- 40- $\mu\text{A}$  Low Quiescent Current at Light Load
- Extreme, Wide ESR Range.
  - Stable with 1- $\mu\text{F}$  to 50- $\mu\text{F}$  Ceramic Output Capacitor, ESR 1 m $\Omega$  to 20  $\Omega$
- Reverse Polarity Protection
- Overtemperature Protection
- Output Short-Circuit Proof to Ground and Supply
- SOT-23 Package

### 2 Applications

- Off-board Sensor Supply
- High-Precision Voltage Tracking

### 3 Description

The TPS7B4250-Q1 device is a monolithic, integrated low-dropout voltage tracker. The device is available in a SOT-23 package. The TPS7B4250-Q1 device is designed to supply off-board sensors in an automotive environment. The IC has integrated protection for overload, over temperature, reverse polarity, and output short-circuit to the battery and ground.

A reference voltage applied at the adjust-input pin, ADJ, regulates supply voltages up to  $V_{\text{IN}} = 45\text{ V}$  with high accuracy and loads up to 50 mA.

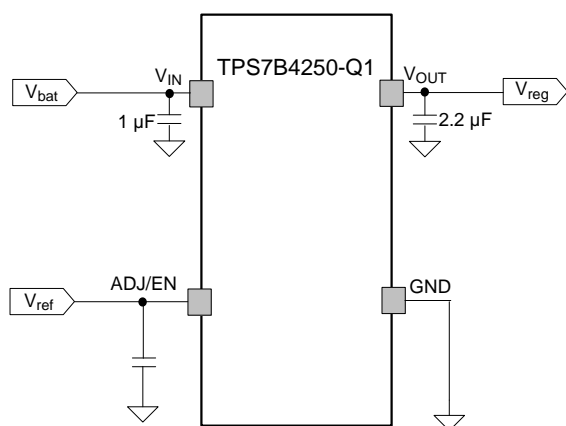
By setting the adjust/enable input pin, ADJ/EN, to low, the TPS7B4250-Q1 device switches to standby mode which reduces the quiescent current to the minimum value.

#### Device Information<sup>(1)</sup>

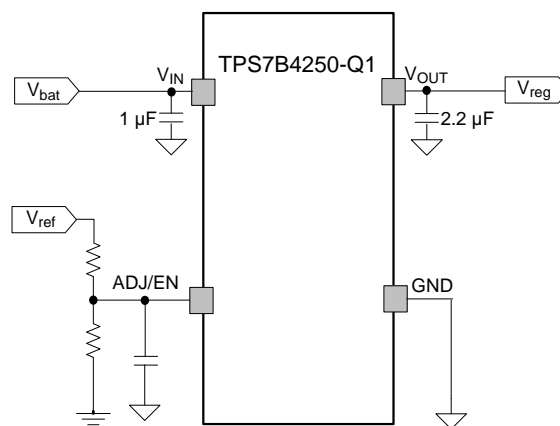
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B4250-Q1	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Output Equal to Reference Voltage



#### Output Lower than Reference Voltage



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision B (July 2015) to Revision C

Page

•	Changed the title of the data sheet .....	1
•	Added the <i>Device Support</i> and <i>Receiving Notification of Documentation Updates</i> sections.....	16

### Changes from Revision A (November 2013) to Revision B

Page

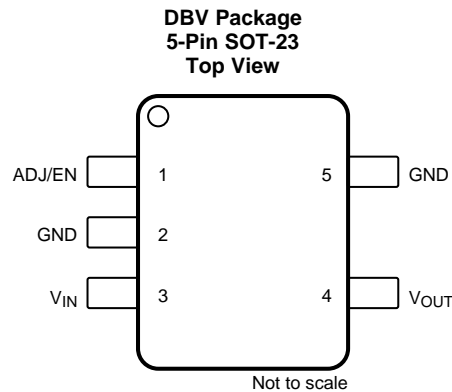
•	Changed HBM ESD Classification level from 2 to 3A .....	1
•	Changed CDM ESD Classification level from C4 to C6 .....	1
•	Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
•	Deleted the transient current and 107-pF capacitor for HBM table notes from the <i>ESD Ratings</i> table .....	5
•	Changed input voltage symbol from $V_{IN}$ to $V_I$ for the $\Delta V_{O(\Delta V)}$ and $V_{dropout}$ parameters and the output voltage symbol from $V_{OUT}$ to $V_O$ for the $I_L$ parameter in the <i>Electrical Characteristics</i> table .....	6
•	Added $I_O$ and $C_O$ to the PSRR test condition in the <i>Electrical Characteristics</i> table .....	6
•	Changed the max value for $V_{dropout}$ where $I_O = 10$ mA from 250 to 265 in the <i>Electrical Characteristics</i> table .....	6
•	Deleted the $V_{ADJ} = 5$ V condition for the <i>Ground current vs Temperature</i> graph and changed the legend.....	7
•	Changed the y axis units from mV to mA in the <i>Current-limit vs Temperature</i> graph .....	7
•	Added the $V_{ADJ}$ condition statement to the <i>Input Voltage vs Output Voltage</i> graph and changed the y-axis from $I_O$ to $V_O$ ..	7
•	Changed the title of <a href="#">Figure 8</a> from <i>Input Voltage vs Output Voltage</i> to <i>Reference Voltage vs Output Voltage</i> , and changed the y-axis from $I_O$ to $V_O$ . Also added the $V_I$ condition statement to the graph.....	7
•	Changed the second y axis from $I_O$ to $V_I$ and removed the units in the <i>Line Transient</i> .....	7
•	Deleted the units from the second y axis in the <i>Load Transient</i> .....	7
•	Added the $V_{ADJ}$ condition statement to the <i>Power-supply Rejection Ratio vs Frequency</i> graph .....	8
•	Added resistor-divider values to the <i>Tracking LDO With Enable Circuit</i> figure.....	11

**Changes from Original (October 2013) to Revision A**
**Page**

• Changed CDM ESD Classification level from C3B to C4 throughout document .....	1
• Changed $V_{OUT}$ min value from $-0.3$ to $-1$ in the <i>Absolute Maximum Ratings</i> table .....	5
• Added transient current flow to ESD rating in the <i>Absolute Maximum Ratings</i> table .....	5
• Changed HBM absolute maximum rating from 2 kV to 4 kV .....	5
• Deleted relevant ESR value from <i>Recommended Operating Conditions</i> table .....	5
• Added grater-than-or-equal-to ( $\geq$ ) value to $V_{ADJ/EN}$ in condition statement of the <i>Electrical Characteristics</i> table .....	6
• Added $V_{ADJ} = 1.5$ V to both test conditions for $V_{UVLO}$ parameter in the <i>Electrical Characteristics</i> table .....	6
• Changed max value for load regulation parameter from 3 to 4 in the <i>Electrical Characteristics</i> table .....	6
• Changed max value for the current consumption test condition where $I_O = 0.5$ mA from 80 to 90 in the <i>Electrical Characteristics</i> table .....	6
• Added the <i>Detailed Description</i> section.....	9
• Added the TPS7B4250 block diagram .....	9

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## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
ADJ/EN	1	I	This pin connects to the reference voltage. A low signal disables the IC and a high signal enables the device. Connected the voltage reference directly or with a voltage divider for lower output voltages. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.
GND	2	G	Internally connected to pin 5
GND	5	G	Internally connected to pin 2
V <sub>IN</sub>	3	I	This pin is the device supply. To compensate for line influences, TI recommends to place a capacitor close to the IC pins.
V <sub>OUT</sub>	4	O	V <sub>OUT</sub> is an external capacitor that is required between V <sub>OUT</sub> and GND with respect to the capacitance and ESR requirements given in the <a href="#">Recommended Operating Conditions</a> .

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Input voltage, unregulated input, $V_{IN}$ <sup>(2)(3)</sup>	-20	45	V
Output voltage, regulated output, $V_{OUT}$	-1	22	V
Adjust input and enable input voltage, ADJ/EN <sup>(2)(3)</sup>	-0.3	22	V
ADJ Voltage minus input voltage ( $ADJ-V_{IN}$ ), $V_{IN} > 0$ V		7	V
Operating junction temperature, $T_J$	-40	150	°C
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground, GND.
- (3) Absolute maximum voltage.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN}$	Unregulated input	4	40	V
$V_{OUT}$	regulated output	1.5	18	V
ADJ/EN	Adjust input and enable input voltage	1.5	18	V
$ADJ-V_{IN}$	ADJ voltage minus input voltage		5	V
$C_{OUT}$	Output capacitor requirements <sup>(2)</sup>	1	50	μF
$ESR_{COUT}$	Output ESR requirements	0.001	20	Ω
$T_J$	Operating junction temperature	-40	150	°C

- (1) Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.
- (2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)(2)</sup>		TPS7B4250-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	4.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
- (2) The thermal data is based on the JEDEC standard high K profile, JESD 51-7. Two-signal, two-plane, four-layer board with 2-oz. copper. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.

## 6.5 Electrical Characteristics

 $V_I = 13.5\text{ V}$ ,  $18\text{ V} \geq V_{ADJ/EN} \geq 1.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO}$	$V_{IN}$ undervoltage detection	Ramp up $V_I$ until the output turns on, $V_{ADJ} = 1.5\text{ V}$	3.65			V
		Ramp down $V_I$ until the output turns off, $V_{ADJ} = 1.5\text{ V}$			3	
$\Delta V_O$	Output-voltage tracking accuracy	$I_O = 100\ \mu\text{A}$ to $1\text{ mA}$ , $V_I = 4\text{ V}$ to $40\text{ V}$ , $1.5\text{ V} < V_{ADJ} < V_I - 0.3\text{ V}$	-4		4	mV
		$I_O = 1\text{ mA}$ to $50\text{ mA}$ , $V_I = 4\text{ V}$ to $40\text{ V}$ , $1.5\text{ V} < V_{ADJ} < V_I - 1.5\text{ V}$	-5		5	
$\Delta V_{O(\Delta I_L)}$	Load regulation steady-state	$I_O = 1\text{ mA}$ to $30\text{ mA}$			4	mV
$\Delta V_{O(\Delta V_I)}$	Line regulation steady-state	$I_O = 10\text{ mA}$ , $V_I = 6\text{ V}$ to $40\text{ V}$			3	mV
PSRR	Power-supply ripple rejection	Frequency = $100\text{ Hz}$ , $V_{rip} = 0.5\text{ V}_{PP}$ , $I_O = 5\text{ mA}$ , $C_O = 2.2\ \mu\text{F}$		60		dB
$V_{dropout}$	Dropout voltage, $V_{dropout} = V_I - V_Q$	$I_O = 10\text{ mA}$ , $V_I \geq 4\text{ V}^{(1)}$		150	265	mV
		$I_O = 50\text{ mA}$ , $V_I \geq 4\text{ V}^{(1)}$		550	1000	
$I_L$	Output-current limitation	$V_O$ short to GND	100		500	mA
$I_R$	Reverse current at $V_{IN}$	$V_I = 0\text{ V}$ , $V_O = 20\text{ V}$ , $V_{ADJ} = 5\text{ V}$	-5		0	$\mu\text{A}$
$I_{RN1}$	Reverse current at negative input voltage	$V_I = -20\text{ V}$ , $V_O = 0\text{ V}$ , $V_{ADJ} = 5\text{ V}$	-5		0	$\mu\text{A}$
$I_{RN2}$		$V_I = -20\text{ V}$ , $V_O = 20\text{ V}$ , $V_{ADJ} = 5\text{ V}$	-5		0	
$T_{SD}$	Thermal shutdown temperature	$T_J$ increasing because of power dissipation generated by the IC		175		$^\circ\text{C}$
$I_Q$	Current consumption	$V_{ADJ} < 0.8\text{ V}$ , $T_A \leq 85^\circ\text{C}^{(2)}$		7.5	15	$\mu\text{A}$
		$V_{ADJ} < 0.8\text{ V}$ , $T_A \leq 125^\circ\text{C}$			20	
		$I_O = 0.5\text{ mA}$ , $V_{ADJ} = 5\text{ V}$		40	90	
		$I_O = 30\text{ mA}$ , $V_{ADJ} = 5\text{ V}$		150	350	
$I_{ADJ}$	Adjust-input and enable-input current	$V_{ADJ} = 5\text{ V}$			1	$\mu\text{A}$
$V_{ADJ,low}$	Adjust and enable low signal valid	$V_O = 0\text{ V}$			0.8	V
$V_{ADJ,high}$	Adjust and enable high signal valid	$ V_O - V_{ADJ}  < 5\text{ mV}$	1.5		18	V

 (1) Measured when the output voltage  $V_Q$  has dropped 10 mV from the typical value.

(2) Ensured by design.

## 6.6 Typical Characteristics

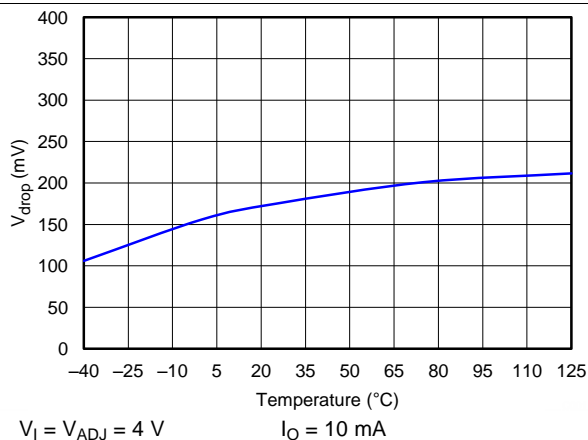


Figure 1. Dropout Voltage vs Temperature

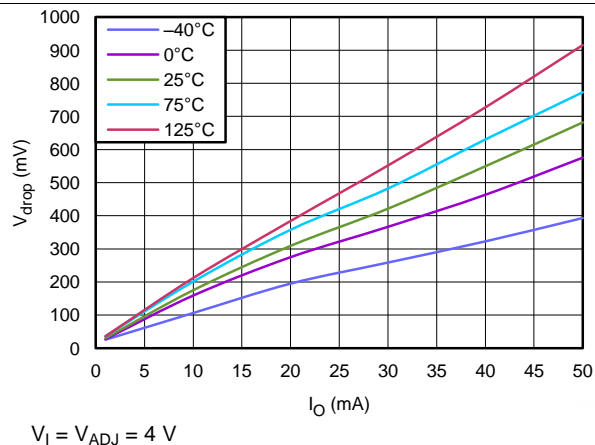


Figure 2. Dropout Voltage vs Output Current

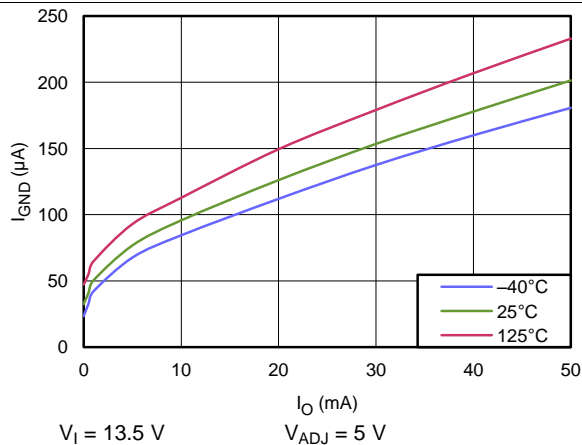


Figure 3. Ground Current vs Output Current

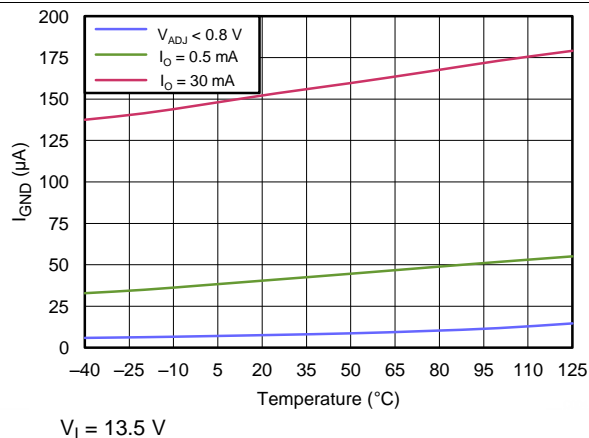


Figure 4. Ground Current vs Temperature

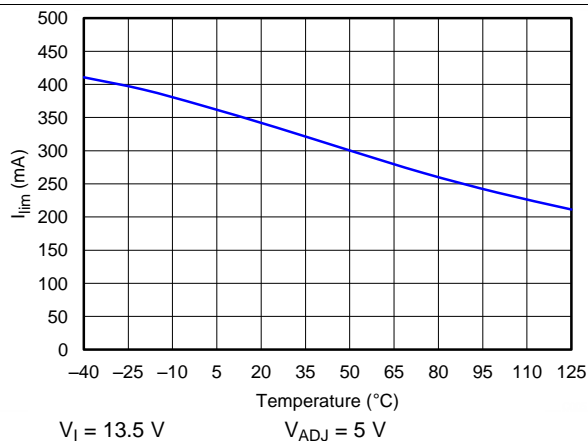


Figure 5. Current-limit vs Temperature

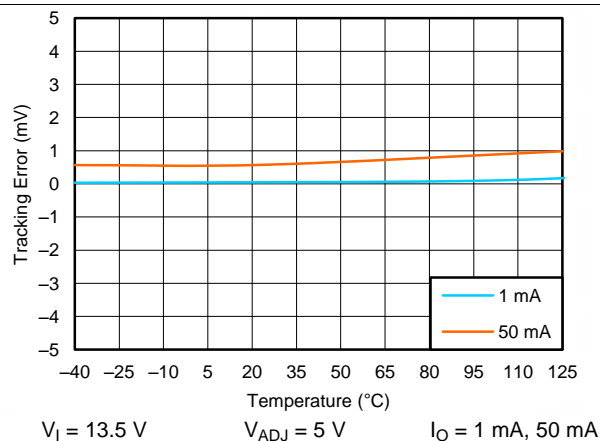


Figure 6. Tracking Error vs Temperature

Typical Characteristics (continued)

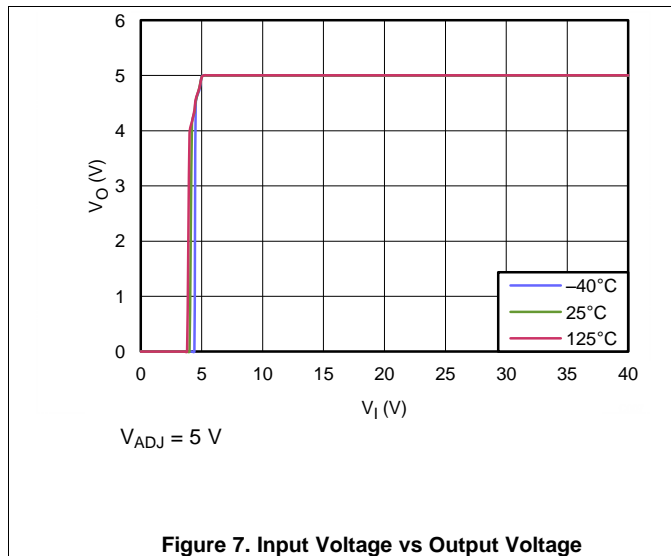


Figure 7. Input Voltage vs Output Voltage

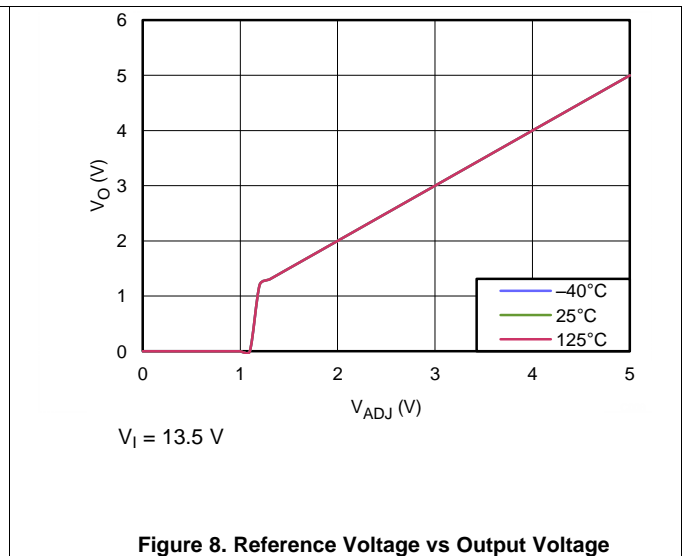


Figure 8. Reference Voltage vs Output Voltage

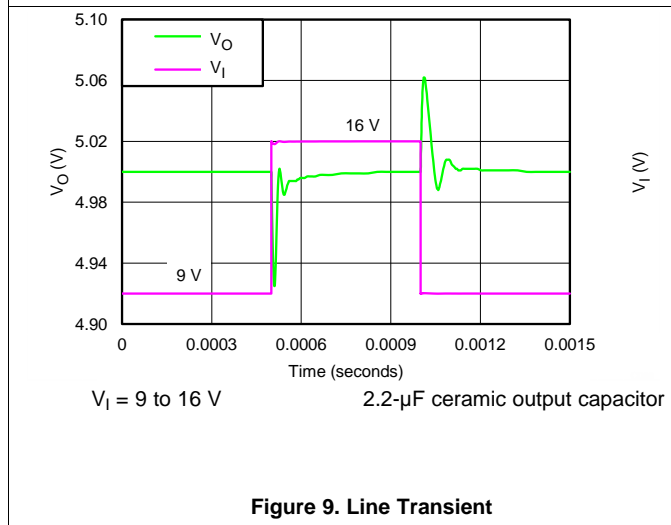


Figure 9. Line Transient

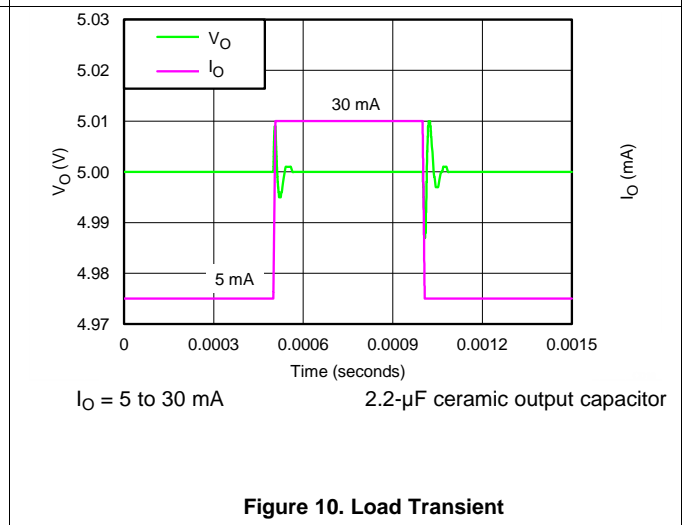


Figure 10. Load Transient

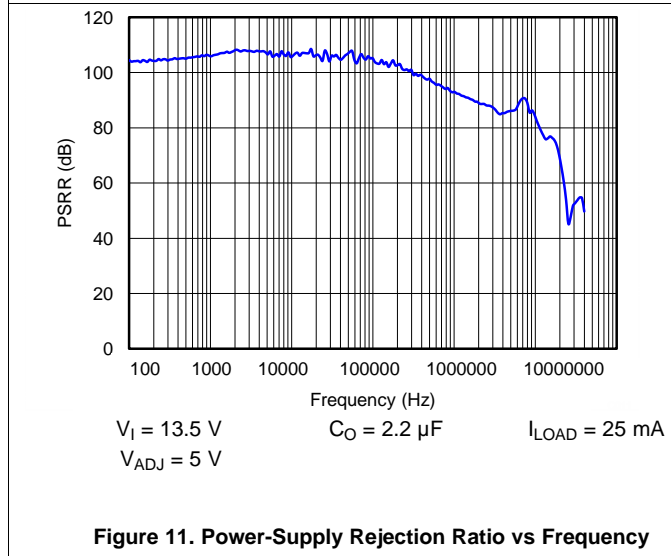


Figure 11. Power-Supply Rejection Ratio vs Frequency

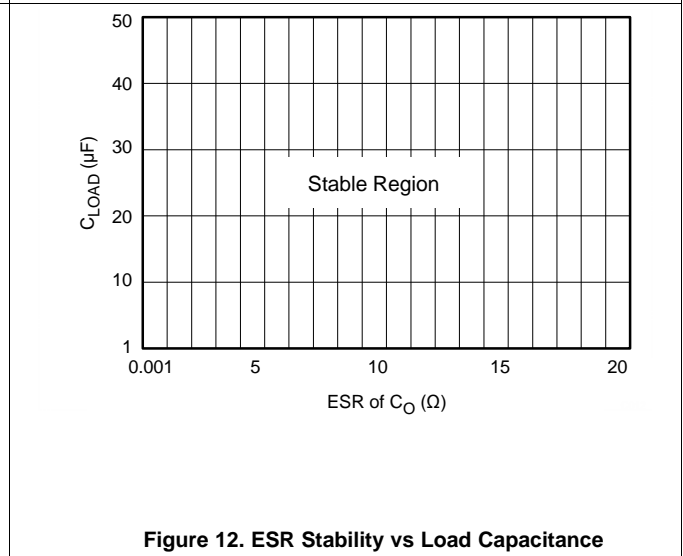


Figure 12. ESR Stability vs Load Capacitance





## Feature Description (continued)

### 7.3.3 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B4250-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B4250-Q1 device into thermal shutdown degrades device reliability.

### 7.3.4 $V_{OUT}$ Short to Battery

The TPS7B4250-Q1 device survives a short to battery when the output is shorted to the battery as shown in Figure 13. No damage occurs to the device. A short to the battery can also occur when the device is powered by an isolated supply at a lower voltage as shown in Figure 14. In this case the TPS7B4250-Q1 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on  $V_{OUT}$  which typically runs at 5 V. The continuous reverse current flows out through  $V_{IN}$  is less than 5  $\mu\text{A}$ .

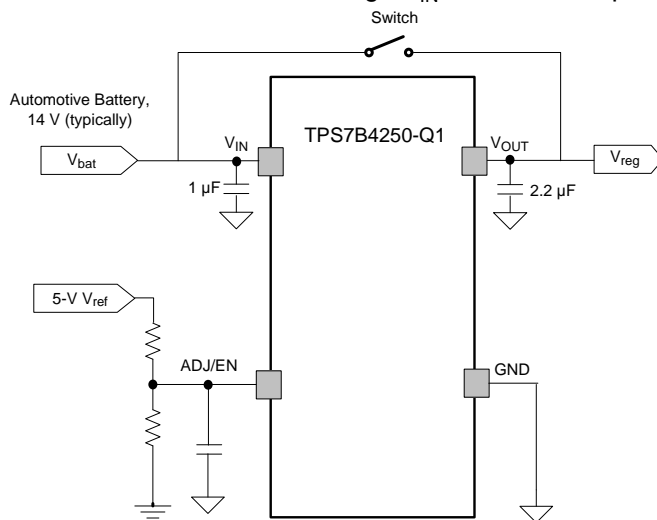


Figure 13. Output-Voltage Short to Battery

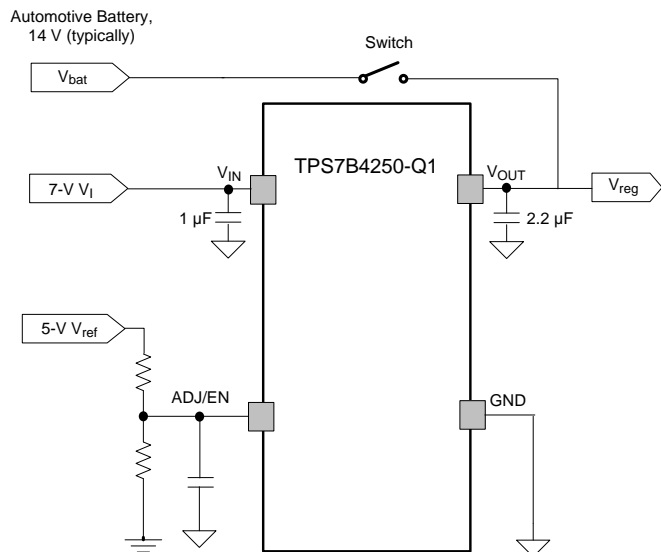


Figure 14. Output Voltage Higher than Input

### 7.3.5 Tracking Regulator with ENABLE Circuit

By pulling the reference voltage of the device below 0.8 V, the IC disables and enters a sleep state where the device draws 7.5  $\mu\text{A}$  (typical) from the power supply. In a real application, the reference voltage is generally sourced from another LDO voltage rail. A case where the device must be disabled without a shutdown of the reference voltage can occur. In such case, the device can be configured as shown in Figure 15. The TPS7A6650-Q1 device is a 150-mA LDO with ultra-low quiescent current that is used as a reference voltage to the TPS7B4250-Q1 device and also as a power supply to the ADC. In a configuration as shown in Figure 15, the status of the device is controlled by an MCU I/O.



## 8 Application and Implementation

### NOTE

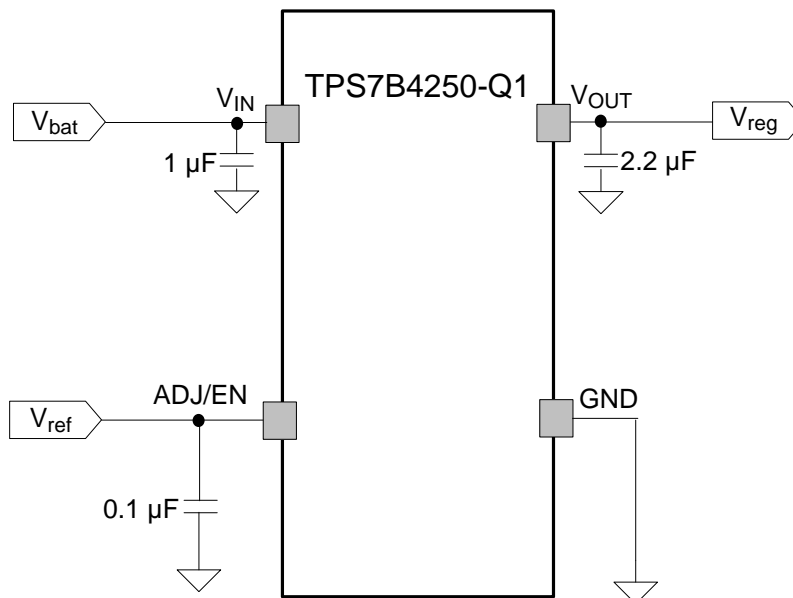
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a reset from occurring. TI recommends a low ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

### 8.2 Typical Application

Figure 16 show typical application circuit for the TPS7B4250-Q1 device.



**Figure 16. Typical Application Schematic**

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	4 to 40 V
ADJ reference voltage	1.5 to 18 V
Output voltage	1.5 to 18 V
Output current rating	50 mA
Output capacitor range	1 µF to 50 µF
Output capacitor ESR range	1 mΩ to 20 Ω

## 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Reference voltage
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

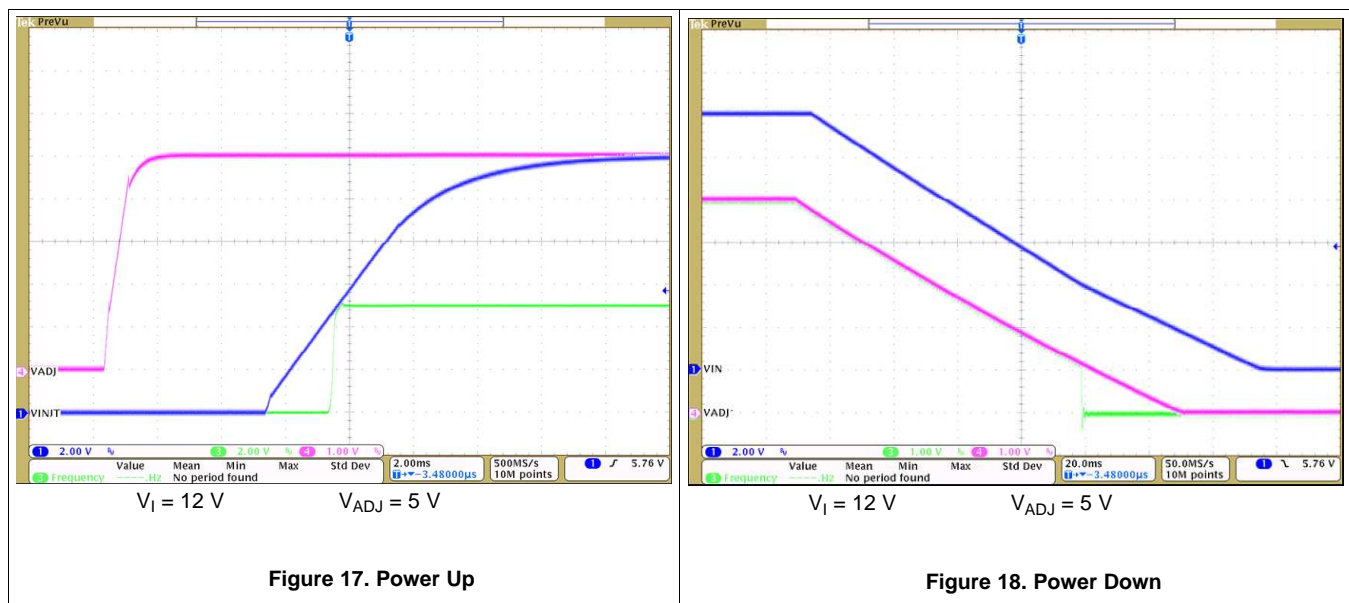
### 8.2.2.1 External Capacitors

An input capacitor,  $C_I$ , is recommended to buffer line influences. Connect the capacitors close to the IC pins.

The output capacitor for the TPS7B4250-Q1 device is required for stability. Without the output capacitor, the regulator oscillates. The actual size and type of the output capacitor can vary based on the application load and temperature range. The effective series resistance (ESR) of the capacitor is also a factor in the IC stability. The worst case is determined at the minimum ambient temperature and maximum load expected. To ensure stability of TPS7B4250-Q1 device, the device requires an output capacitor between 1  $\mu\text{F}$  and 50  $\mu\text{F}$  with an ESR range between 0.001  $\Omega$  and 20  $\Omega$  that can cover most types of capacitor ESR variation under the recommend operating conditions. As a result, the output capacitor selection is flexible.

The capacitor must also be rated at all ambient temperature expected in the system. To maintain regulator stability down to  $-40^\circ\text{C}$ , use a capacitor rated at that temperature.

## 8.2.3 Application Curves



## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B4250-Q1 device, adding an electrolytic capacitor with a value of 10- $\mu\text{F}$  and a ceramic bypass capacitor at the input is recommended.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4250-Q1 device are available in the [Mechanical, Packaging, and Orderable Information](#) section and at [www.ti.com](http://www.ti.com).

#### 10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7B4250 evaluation board, available at [www.ti.com](http://www.ti.com).

### 10.2 Layout Example

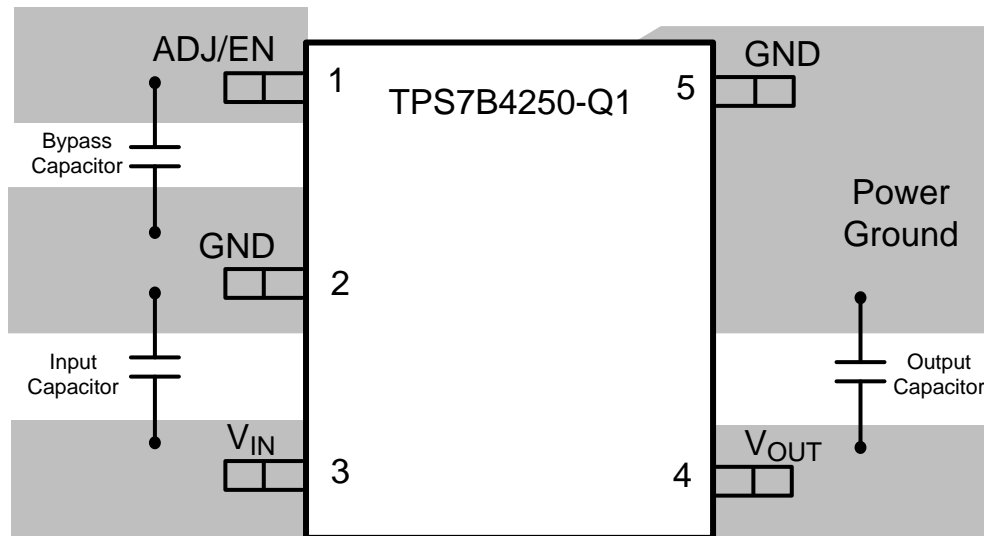


Figure 19. TPS7B4250-Q1 Layout Example

### 10.3 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with [Equation 1](#).

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- $P_D$  = continuous power dissipation
- $I_O$  = output current
- $V_I$  = input voltage
- $V_O$  = output voltage
- $I_Q$  = quiescent current

(1)

As  $I_Q \ll I_O$ , the term  $I_Q \times V_I$  in [Equation 1](#) can be ignored.

For a device under operation at a given ambient air temperature ( $T_A$ ), calculate the junction temperature ( $T_J$ ) with [Equation 2](#).

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where

- $\theta_{JA}$  = junction-to-junction-ambient air thermal impedance

(2)

A rise in junction temperature because of power dissipation can be calculated with [Equation 3](#).

$$\Delta T = T_J - T_A = (\theta_{JA} \times P_D)$$

(3)

For a given maximum junction temperature ( $T_{JM}$ ), the maximum ambient air temperature ( $T_{AM}$ ) at which the device can operate can be calculated with [Equation 4](#).

$$T_{AM} = T_{JM} - (\theta_{JA} \times P_D)$$

(4)

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

For the PSpice model, see the [TPS7B4250 PSpice Transient Model](#) (SLV976).

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [Various Applications for Voltage-Tracking LDO](#) (SLVA789)
- [TPS7B4250 Evaluation Module](#) (SLVU975)
- [TPS7B4250-Q1 Pin FMEA](#) (SLVA738)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B4250QDBVQ1	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 125		
TPS7B4250QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PA3Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

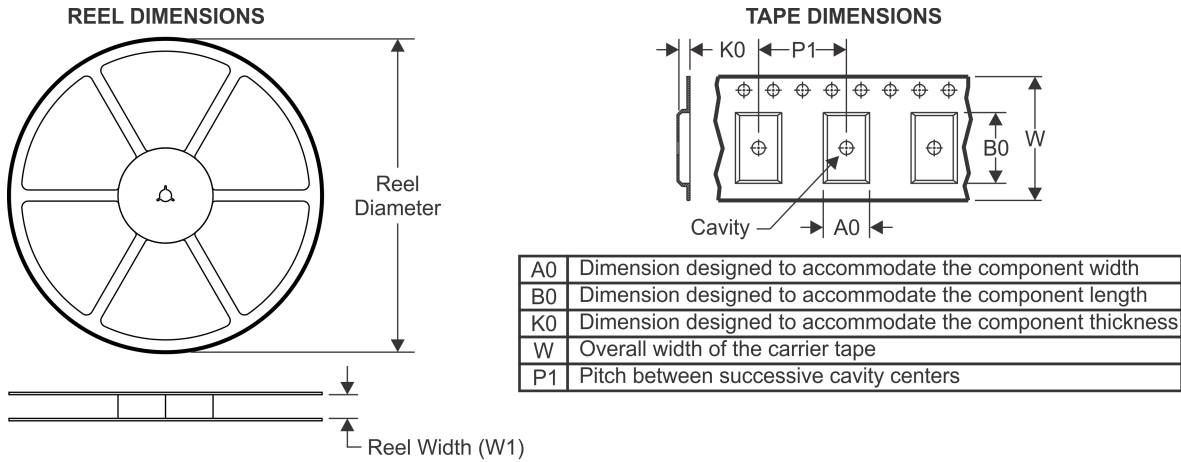
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

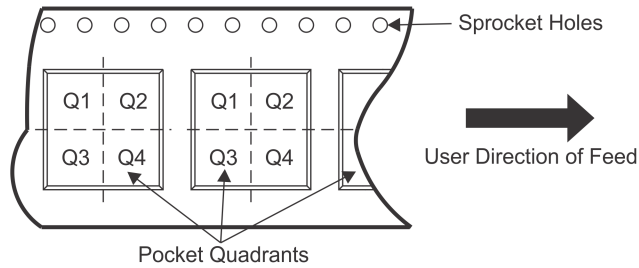
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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B4250QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B4250QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0

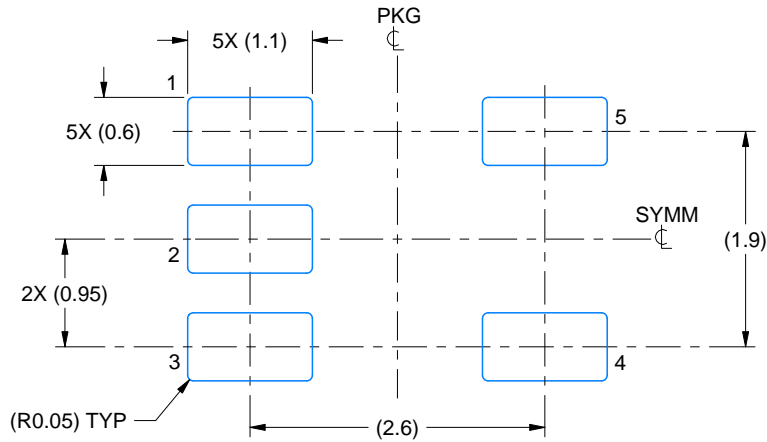


# EXAMPLE BOARD LAYOUT

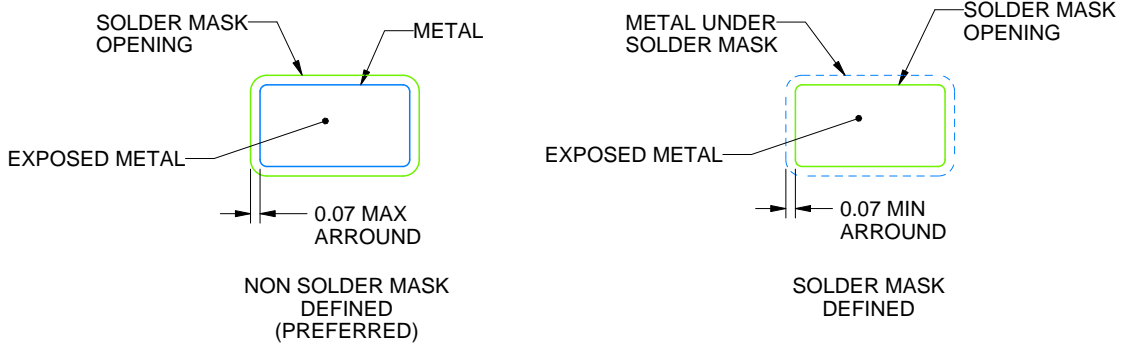
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

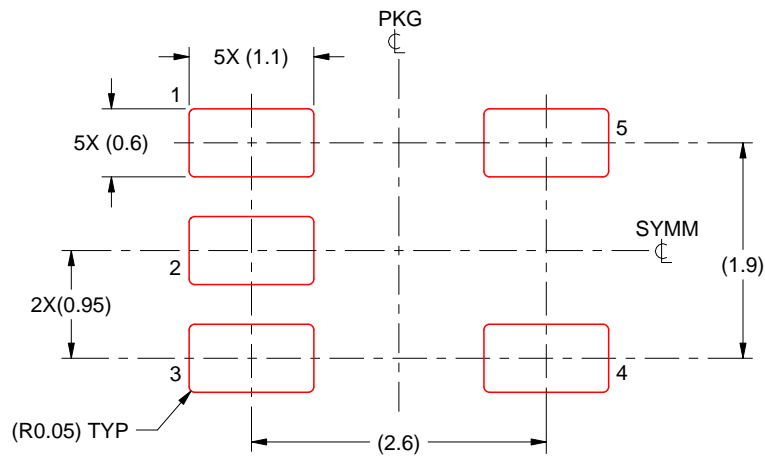
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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