MC33765

Very Low Dropout/Ultra Low Noise 5 Outputs Voltage Regulator

The MC33765 is an ultra low noise, very low dropout voltage regulator with five independent outputs which is available in TSSOP−16 surface mount package.

The MC33765 is available in 2.8 V. The output voltage is the same for all five outputs but each output is capable of supplying different currents up to 150 mA for output 4. The device features a very low dropout voltage (0.11 V typical for maximum output current), very low quiescent current (5.0 μA maximum in OFF mode, 130 μA typical in ON mode) and one of the output (output 3) exhibits a very low noise level which allows the driving of noise sensitive circuitry. Internal current and thermal limiting protections are provided.

Additionally, the MC33765 has an independent Enable input pin for each output. It includes also a common Enable pin to shutdown the complete circuit when not used. *The Common Enable pin has the highest priority over the five independent Enable input pins.*

The voltage regulators VR1, VR2 and VR3 have a common input voltage pin $V_{CC}1$. The other voltage regulators VR4 and VR5 have a common input voltage pin $V_{CC}2$.

Features

- Five Independent Outputs at 2.8V Typical, Based Upon Voltage Version
- Internal Trimmed Voltage Reference
- V_{out} Tolerance ±3.0% over the Temperature Range −40°C to +85°C
- Enable Input Pin (Logic−Controlled Shutdown) for Each of the Five Outputs
- Common Enable Pin to Shutdown the Whole Circuit
- Very Low Dropout Voltage (0.11 V Typical for Output 1, 2, 3 and 5; 0.17 V Typical for Output 4 at Maximum Current)
- Very Low Quiescent Current (Maximum 5.0 μA in OFF Mode, 130 μA Typical in ON Mode)
- Ultra Low Noise for VR3 (30 μV RMS Max, 100 Hz < f < 100 kHz)
- Internal Current and Thermal Limit
- 100 nF for VR1, VR2, VR4 and VR5 and 1.0 μF for VR3 for Stability
- Supply Voltage Rejection: 60 dB (Typical) @ f = 1.0 kHz
- These are Pb−Free Devices*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	5.3	V
Thermal Resistance Junction−to−Air	$R_{\theta JA}$	140	°C/W
Operating Ambient Temperature	T_A	−40 to +85	°C
Maximum Operating Junction Temperature	T_J	125	°C
Maximum Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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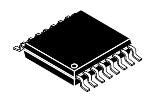
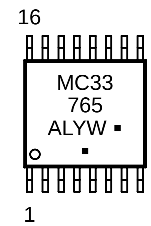
MARKING DIAGRAM

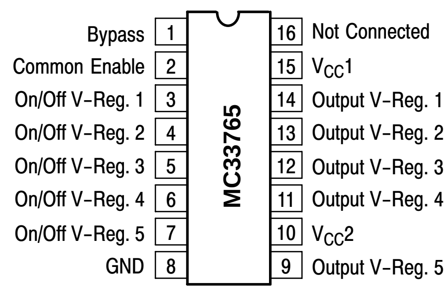


TSSOP−16
DTB SUFFIX
CASE 948F



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

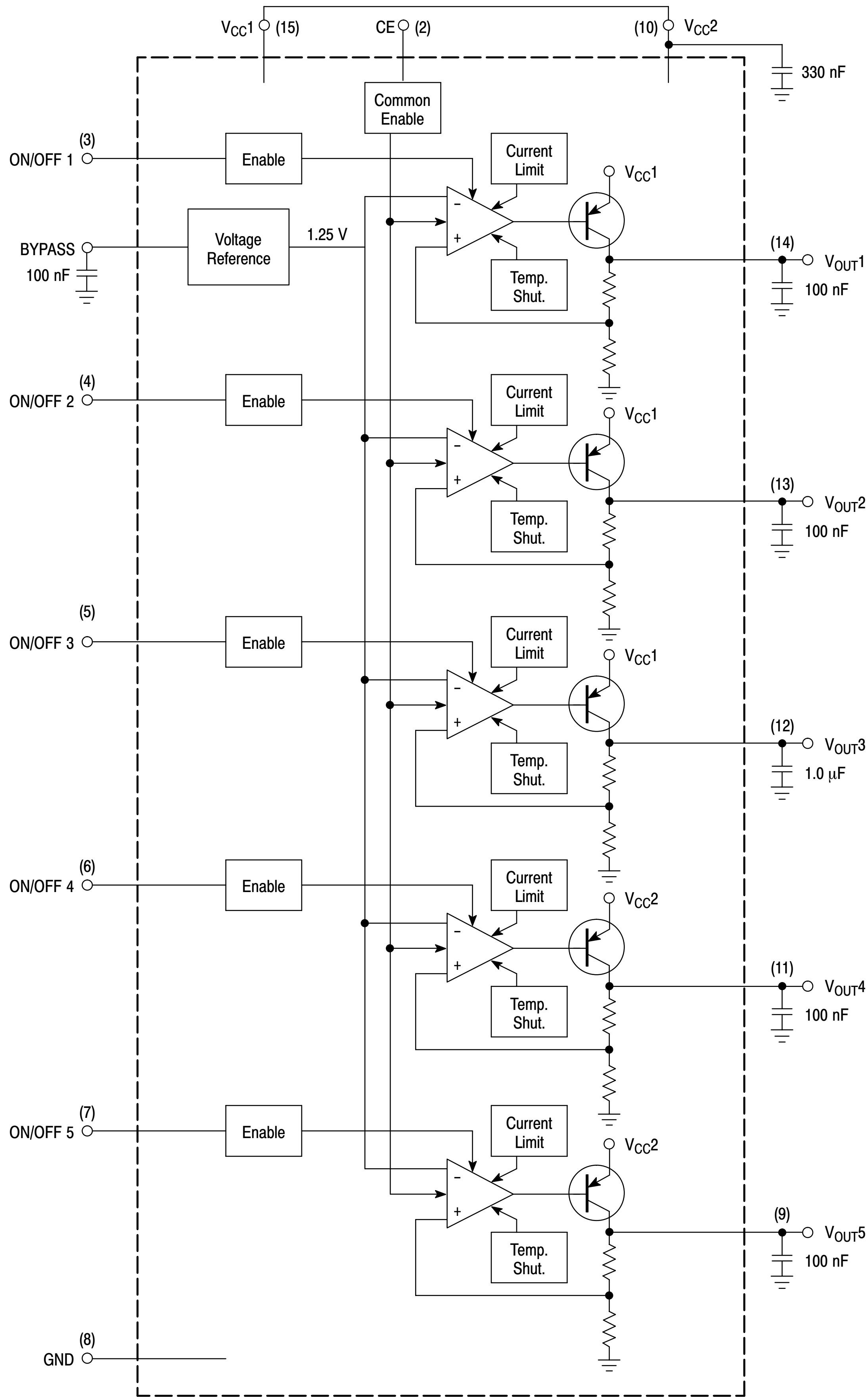
Device	Package*	Shipping†
MC33765DTB	TSSOP−16	96 Units/Rail
MC33765DTBG	TSSOP−16	96 Units/Rail
MC33765DTBR2	TSSOP−16	2500 Tape & Reel
MC33765DTBR2G	TSSOP−16	2500 Tape & Reel

*This package is inherently Pb−Free.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Simplified Block Diagram



CONTROL ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C/ Max T_J = 125°C)

Characteristics	Symbol	Pin #	Min	Typ	Max	Unit
INDEPENDENT ENABLE PINS						
Input Voltage Range	$V_{ON/OFF(1-5)}$	−	0	−	V_{CC}	V
Control Input Impedance		−	100	−	−	kΩ
Logic “0”, i.e. OFF State Logic “1”, i.e. ON State	$V_{ON/OFF(1-5)}$	−	− 2.0	− −	0.5 −	V
COMMON ENABLE PIN						
Input Voltage Range	V_{CE}	2	0	−	V_{CC}	V
Control Input Impedance		2	100	−	−	kΩ
Logic “0”, i.e. OFF State Logic “1”, i.e. ON State	V_{CE}	2	− 2.0	− −	0.3 −	V
CURRENT CONSUMPTION WITH NO LOAD						
Current Consumption at Logic “0” for the complete device, i.e. Common Enable and All Independent Enable pins at OFF State	IQ_{OFF}		−	−	5.0	μA
Current Consumption at Logic “1” for the complete device, i.e. Common Enable and All Independents Enable pins at ON State	IQ_{ON1}		−	470	−	μA
Current Consumption at Logic “1”, Common Enable at ON State and All Independents Enable pins at OFF State	IQ_{ON2}		−	130	−	μA
SUPPLY AND OUTPUT VOLTAGES, DROPOUT AND LOAD REGULATION						
Supply Voltage V_{CC} MC33765 (2.8V)	V_{CC1}, V_{CC2}	15, 10	3.0	3.6	5.3	V
Regulator Output Voltage for VR1, VR2, VR3, VR4 and VR5 MC33765 (2.8V)	$V_{OUT(1-5)}$	14, 13, 12, 11, 9	2.7	2.8	2.85	V
Dropout Voltage for VR1, VR2, VR3, VR5 (Note 1)	$V_{CC}-V_{OUT}$	14, 13, 12, 9	−	0.11	0.17	V
Dropout Voltage for VR4 (Note 1)	$V_{CC}-V_{OUT4}$	11	−	0.17	0.30	V
Load Regulation (T_A = 25°C)	$Reg_{load(1-5)}$	9, 11, 12, 13, 14	−	−	0.5	mV/mA
MAX POWER DISSIPATION AND TOTAL DC OUTPUT CURRENT (VR1 + VR2 + VR3 + VR4 + VR5) (Note 2)						
Max Power Dissipation at V_{CC} = 5.3 V (T_A = 85°C) Max. Total RMS Output Current at V_{CC} = 5.3 V (T_A = 85°C)	P_{dmax} I_{RMS}	−	− −	− −	285 130	mW mA
Max Power Dissipation at V_{CC} = 5.3 V (T_A = 25°C) Max. Total RMS Output Current at V_{CC} = 5.3 V (T_A = 25°C)	P_{dmax} I_{RMS}	−	− −	− −	700 250	mW mA

1. Typical dropout voltages have been measured at currents: Output1: 25 mA, Output2: 35 mA, Output3: 40 mA, Output4: 140 mA, Output5: 40 mA Maximum value of dropout voltages are measured at maximum specified current.
2. See package power dissipation and thermal protection.

REGULATOR ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C/ Max T_J = 125°C)

Characteristics	Pin #	Symbol	Min	Typ	Max	Unit
OUTPUT CURRENTS (Note 3)						
Regulator VR1 Output Current	14	I_{OUT1}	10	−	30	mA
Regulator VR2 Output Current	13	I_{OUT2}	10	−	40	mA
Regulator VR3 Output Current	12	I_{OUT3}	0	−	50	mA
Regulator VR4 Output Current	11	I_{OUT4}	10	−	150	mA
Regulator VR5 Output Current	9	I_{OUT5}	10	−	60	mA
Current Limit for VR1, VR2, VR3, VR4, VR5 [Twice the max Output Current for each output]	14, 13, 12, 11, 9	I_{MAX}	−	2 X I_{OUT} (1−5)	−	mA
EXTERNAL CAPACITORS						
External Compensation Capacitors for VR1, VR2, VR4, VR5	14, 13, 11, 9	$C_{(1-2,\ 4-5)}$	0.10	−	1.0	μF
External Compensation Capacitors for VR3	12	C_4	1.0	−	−	μF
External Compensation Capacitors ESR	−	−	0.05	1.0	3.0	Ω
RIPPLE REJECTIONS						
Ripple Rejection VR1, VR2, VR4, VR5 (at Max. Current, 1.0 kHz, C = 100 nF)	14, 13, 11, 9	$\frac{(\Delta V_{OUT})}{(\Delta V_{CC})}$	50	60	−	dB
Ripple Rejection VR1, VR2, VR4, VR5 (at Max. Current, f = 10 kHz, C = 100 nF)	14, 13, 11, 9	$\frac{(\Delta V_{OUT})}{(\Delta V_{CC})}$	40	45	−	dB
Ripple Rejection of VR3 (at Max. Current, f = 1.0 kHz, C = 1.0 μF)	12	$\frac{(\Delta V_{OUT})}{(\Delta V_{CC})}$	50	60	−	dB
Ripple Rejection of VR3 (at Max. Current, f = 10 kHz, C = 1.0 μF)	12	$\frac{(\Delta V_{OUT})}{(\Delta V_{CC})}$	40	45	−	dB
Ripple Rejection of VR3 (at Max. Current, f = 100 kHz, C = 1.0 μF)	12	$\frac{(\Delta V_{OUT})}{(\Delta V_{CC})}$	18	22	−	dB
DYNAMIC PARAMETERS						
Rise Time (1% → 99%) Common Enable at ON state, C_{bypass} = 10 nF, I_{out} at max. current VR1, VR2, VR4, VR5 with C_{OUT} = 100 nF, T_A = 25°C VR3 with C_{OUT} = 1.0 μF, T_A = 25°C		t_{on}	 − −	 − −	 30 150	 μs μs
Fall Time (99% → 1%) [C_{OUT} = 100 nF, I_{OUT} = 30 mA] (Note 4)		t_{off}	−	100	−	μs
Overshoot (C_{OUT} = 100 nF for VR1, VR2, VR4, VR5 and C_{OUT} = 1.0 μF for VR3) at T_A = 25°C Common Enable at ON state, independent enable from OFF to ON state		−	−	5	8	%
Settling Time (to ±0.1% of nominal) at T_A = 25°C Common Enable at ON state, independent enable from OFF to ON state		−	−	95	−	μs
NOISE AND CROSSTALKS						
Noise Voltage (100 Hz < f < 100 kHz) with C_{bypass} = 100 nF VR1, VR2, VR4, VR5 with C_{OUT} = 100 nF; VR3 with C_{OUT} = 1.0 μF		−	− −	40 25	− 30	μV RMS
Static crosstalk (DC shift) between the Regulator Output, T_A = 25°C (Note 5)		−	−	150	200	μV
Dynamic CrossTalk Attenuation between the Regulator Outputs (f = 10 kHz), T_A = 25°C (Note 6)		−	30	35	−	dB
THERMAL SHUTDOWN						
Thermal Shutdown		−	−	160	−	°C

3. Maximum Output Currents are peak values. Total DC current have to be set upon maximum power dissipation specification. Only Output 3 has been designed to be stable at minimum current of 0 mA.
4. The Fall time is highly dependent on the load conditions, i.e. load current for a specified value of C_{OUT}.
5. Static Crosstalk is a DC shift caused by switching ON one of the outputs through independent enable to all other outputs. This parameter is highly dependent on overall PCB layout and requires the implementation of low−noise GROUND rules (e.g. Ground plane).
6. Dynamic crosstalk is the ratio between a forced output signal to signal transferred to other outputs. This requires special device configuration to be measured.

MC33765 TYPICAL OSCILLOSCOPE SHOTS

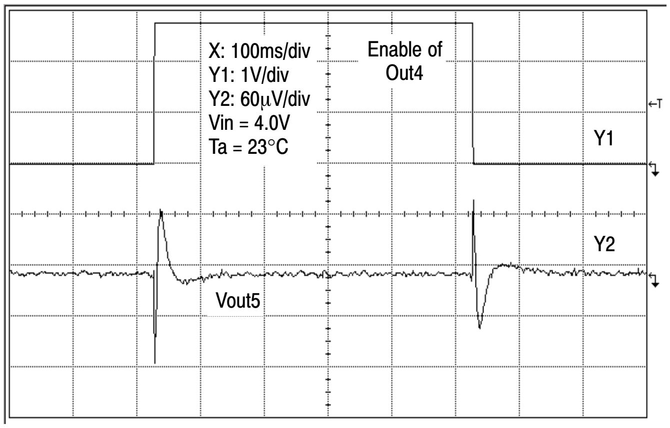


Figure 1. Crosstalk response of MC33765 showing extremely weak interaction between outputs Output 4 is banged from 0 to 150mA

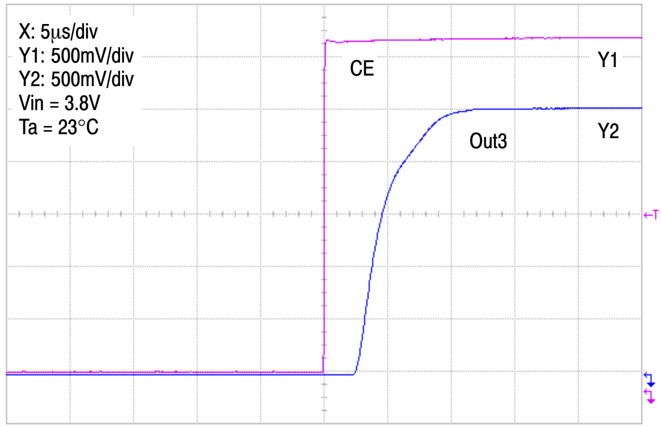


Figure 2. Repetitive Common Enable response time

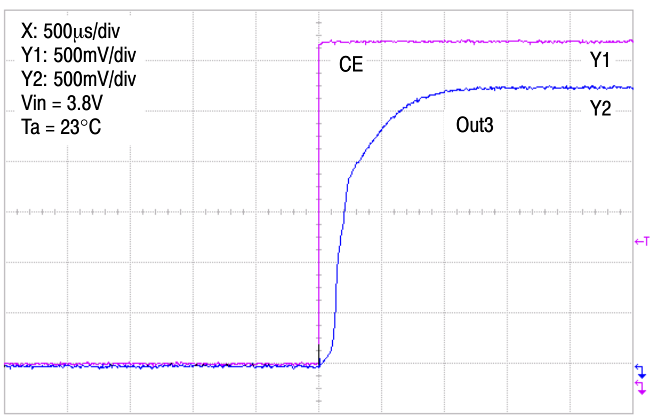


Figure 3. Single Common Enable response time (Cbypass discharged)

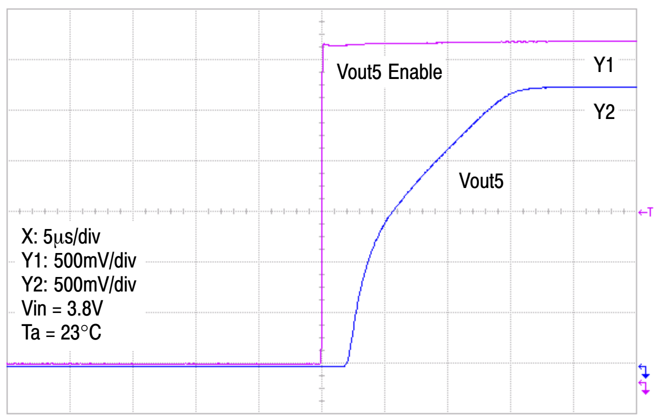


Figure 4. Output response from seperate Enable

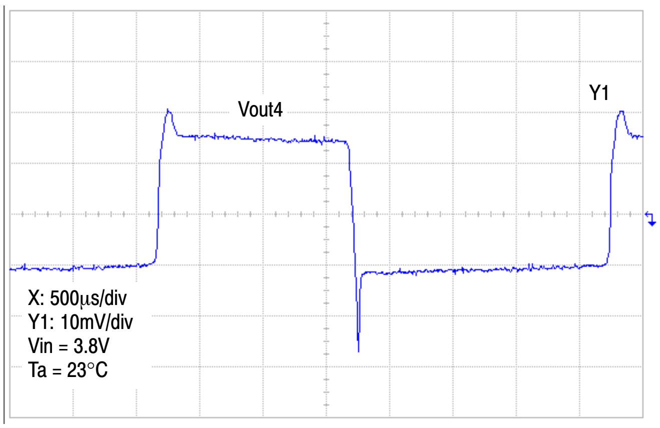


Figure 5. Output 4 is banged from 3mA to 150mA

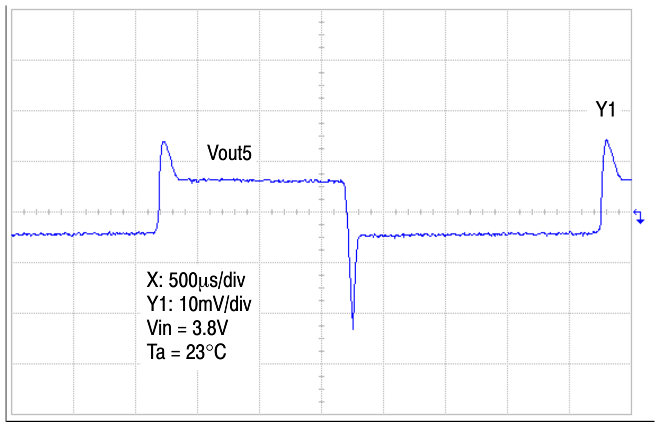


Figure 6. Output 5 is banged from 3mA to 50mA

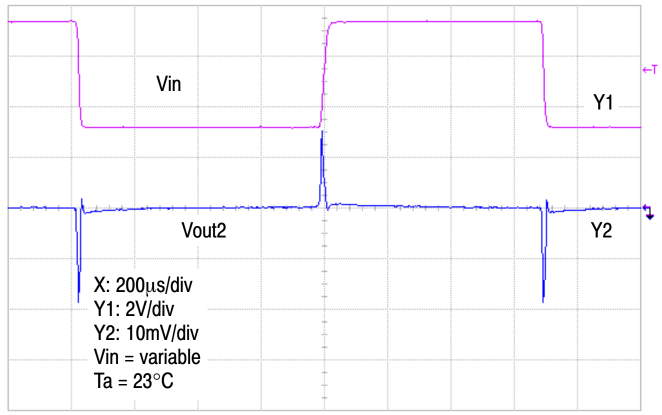


Figure 7. Typical input voltage rejection (Cout = 100nF)

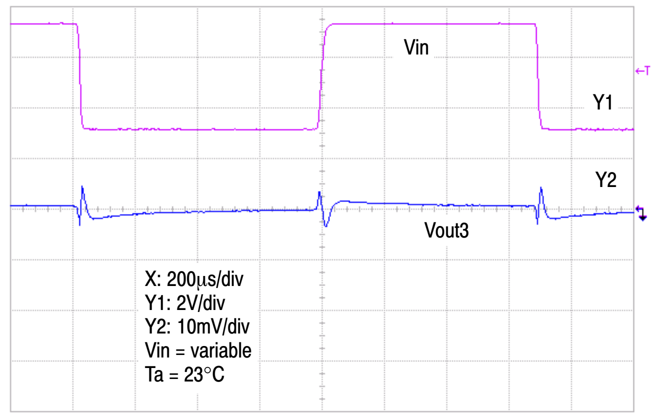


Figure 8. Typical input voltage rejection (Cout = 1µF)

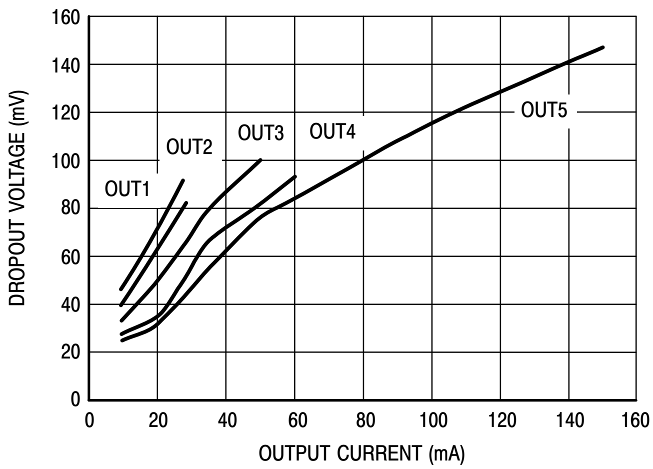


Figure 9. Dropout Voltage versus Output Current

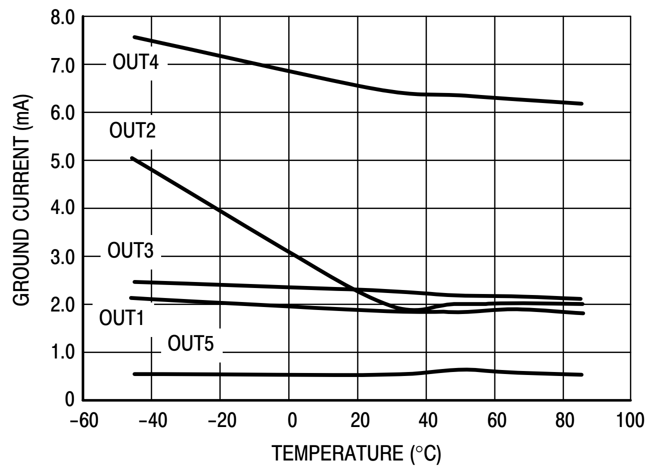


Figure 10. Ground Current versus Individual Output

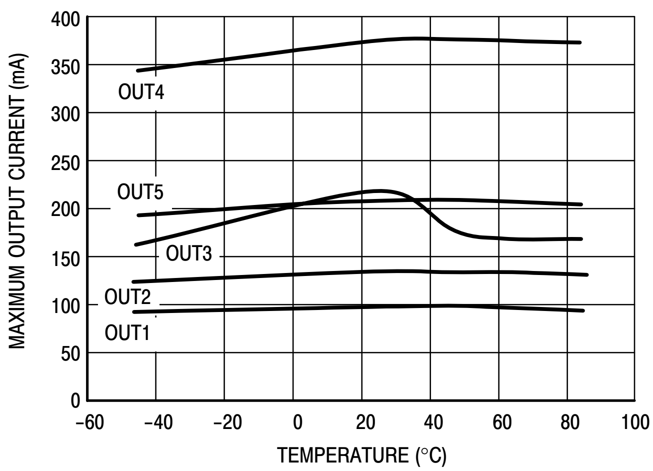


Figure 11. Maximum Output Current versus Temperature

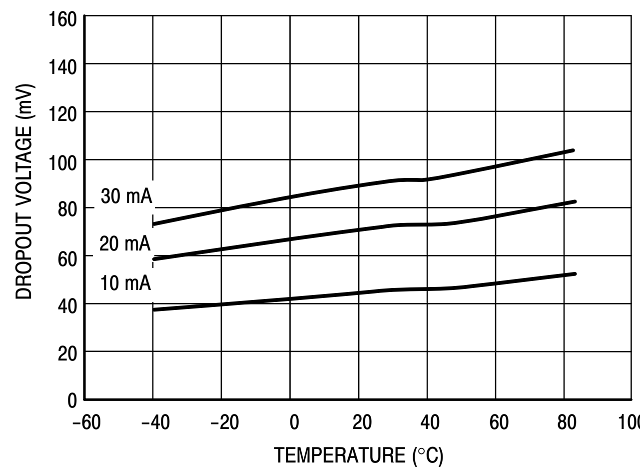


Figure 12. Dropout Voltage versus Operating Temperature: OUT1

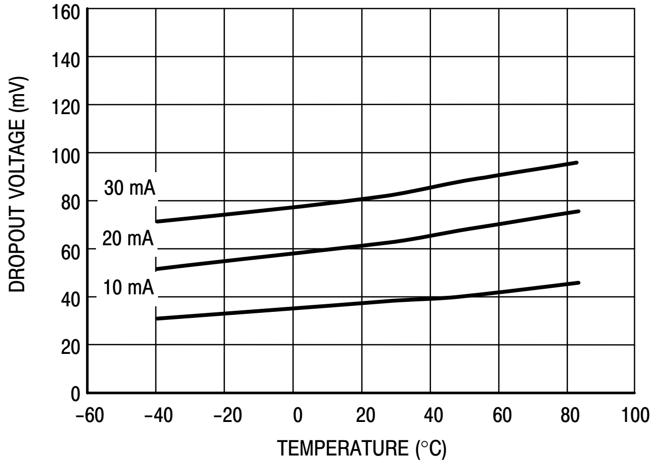


Figure 13. Dropout Voltage versus Operating Temperature: OUT2

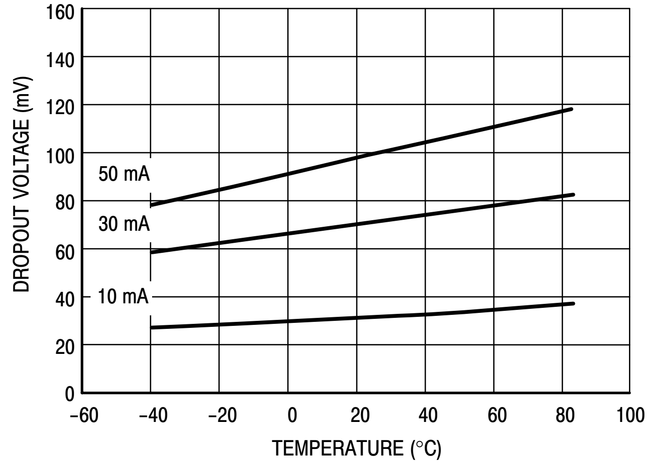


Figure 14. Dropout Voltage versus Operating Temperature: OUT3

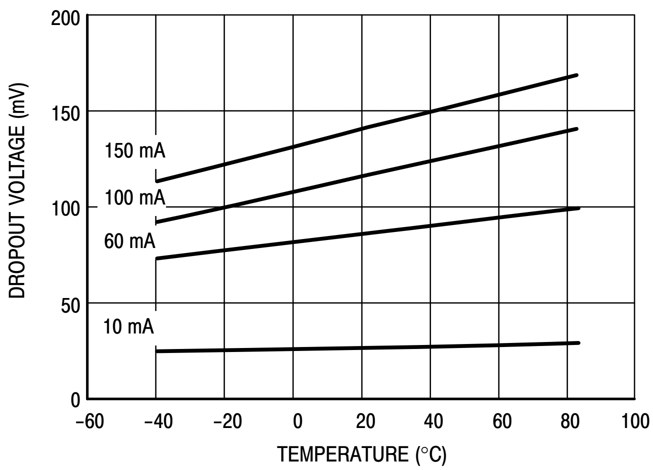


Figure 15. Dropout Voltage versus Operating Temperature: OUT4

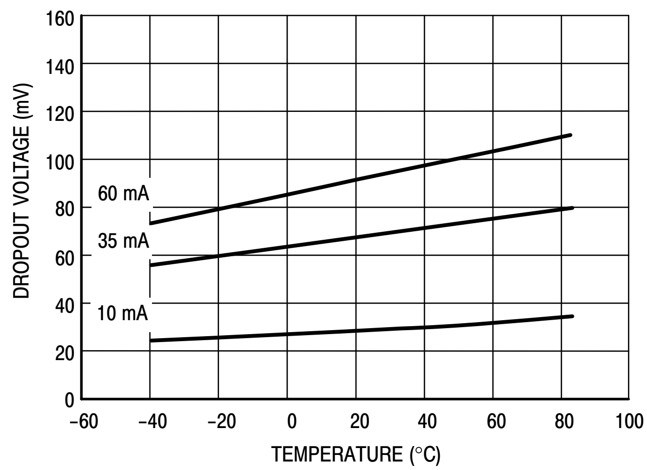


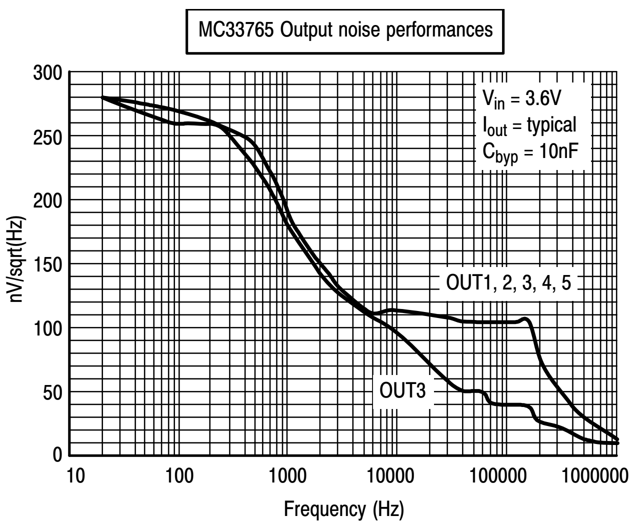
Figure 16. Dropout Voltage versus Operating Temperature: OUT5

DEFINITIONS

Load Regulation − The change in output voltage for a change in load current at constant chip temperature.

Dropout Voltage − The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential input/output), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Output Noise Voltage − The RMS AC voltage at the output with a constant load and no input ripple, measured over a specified frequency range.



Maximum Power Dissipation − The maximum total dissipation for which the regulator will operate within specifications.

Quiescent Current − Current which is used to operate the regulator chip with no load current.

Line Regulation − The change in input voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Thermal Protection − Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically 160°C, the regulator turns off. This feature is provided to prevent catastrophic failures from accidental overheating.

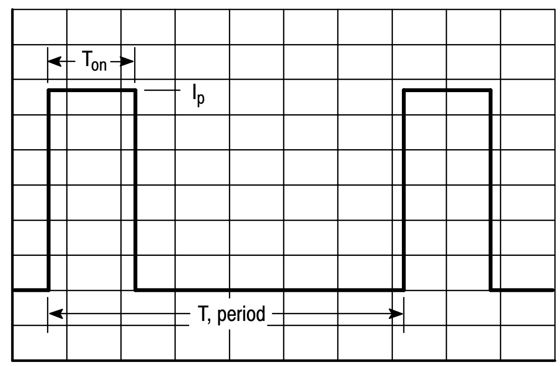
Maximum Package Power Dissipation and RMS Current − The maximum package power dissipation is the power dissipation level at which the junction temperature reaches its maximum value i.e. 125°C. The junction temperature is rising while the difference between the input power (V_{CC} X I_{CC}) and the output power (V_{out} X I_{out}) is increasing.

As MC33765 device exhibits five independent outputs I_{out} is specified as the maximum RMS current combination of the five output currents.

As the device can be switched ON/OFF through independent Enable (ON/OFF pin) or Common Enable, the output signal could be, for example, a square wave. Let’s assume that the device is ON during T_{ON} on a signal period T. The RMS current will be given by:

$$I_{out_{RMS}} = I_P \times \sqrt{D}$$

where $$D = \frac{T_{ON}}{T}$$



Depending on ambient temperature, it is possible to calculate the maximum power dissipation and so the maximum RMS current as following:

$$Pd = \frac{T_J - T_A}{R_{\theta JA}}$$

The maximum operating junction temperature T_J is specified at 125°C, if T_A = 25°C, then P_D = 700 mW. By neglecting the quiescent current, the maximum power dissipation can be expressed as:

$$I_{out} = \frac{P_D}{V_{CC} - V_{out}}$$

So that in the more drastic conditions:

V_{CC} = 5.3 V, V_{out} = 2.7 V then the maximum RMS value of I_{out} is 269 mA.

The maximum power dissipation supported by the device is a lot increased when using appropriate application design. Mounting pad configuration on the PCB, the board material and also the ambient temperature are affected the rate of temperature rise. It means that when the I_C has good thermal conductivity through PCB, the junction temperature will be “low” even if the power dissipation is great.

The thermal resistance of the whole circuit can be evaluated by deliberately activating the thermal shutdown of the circuit (by increasing the output current or raising the input voltage for example).

Then you can calculate the power dissipation by subtracting the output power from the input power. All variables are then well known: power dissipation, thermal shutdown temperature (160°C for MC33765) and ambient temperature.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D}$$

DESIGN HINTS
Reducing the cross−talk between the MC33765 outputs

One of the origin of the DC shift finds its seat in the layout surrounding the integrated circuit. Particular care has to be taken when routing the output ground paths. Star grounding or a ground plane are the absolute conditions to reduce the noise or shift associated to common impedance situations, as depicted by Figure 17.

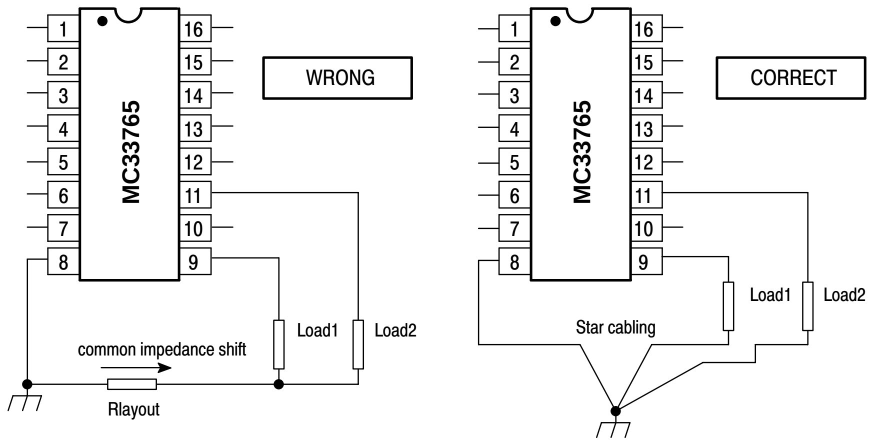


Figure 17. Star Cabling Avoids Coupling by Common Ground Impedance

The first left cabling will generate a voltage shift which will superimpose on the output voltages, thus creating an undesirable offset. By routing the return grounds to a single low impedance point, you naturally shield the circuit against common impedance disturbances. Figure 18 portraits the text fixture implemented to test the response of the MC33765.

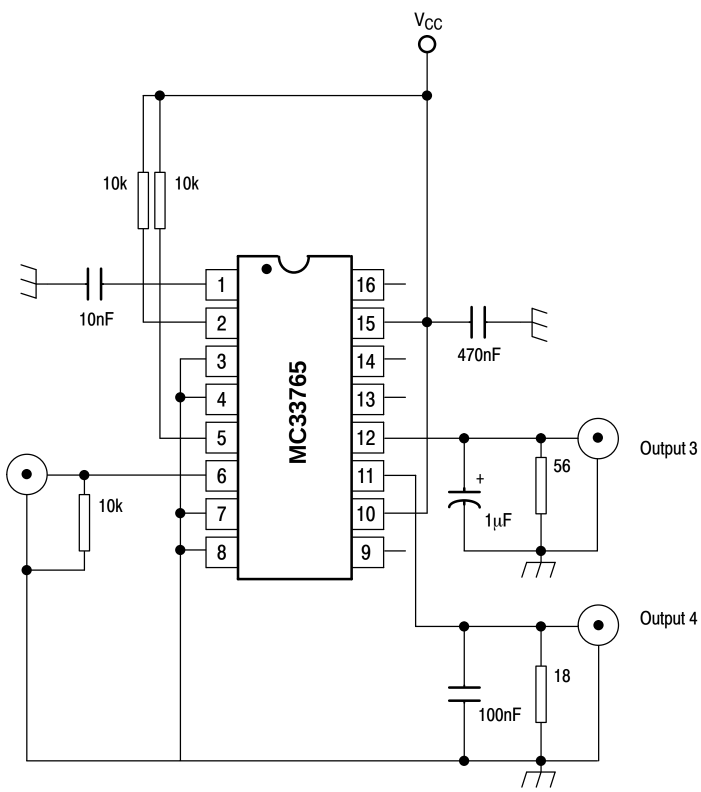


Figure 18. DC Shift Text Fixture

DESIGN HINTS (cont.)

Output 4 was banged from 0 to 150mA via its dedicated control pin, while output 3 fixed at 50mA was monitored. The circuit has been implemented on a PCB equipped with a ground plane and routed with short copper traces. The results are shown hereafter, revealing the excellent behavior of the MC33765 when crosstalks outputs is at utmost importance.

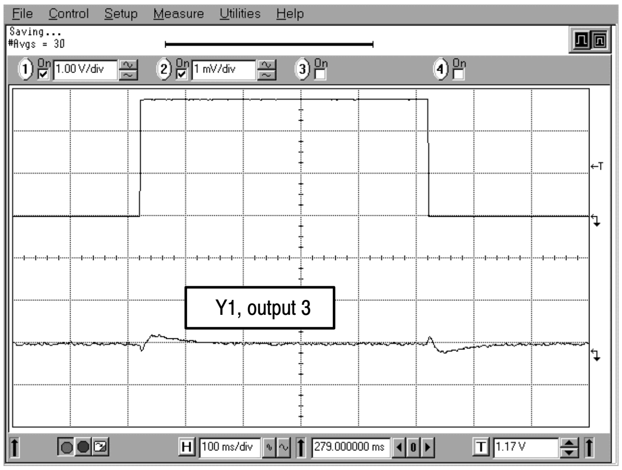


Figure 19. Vin = 4V, Y1 = 62.5μV/div, F = 200Hz

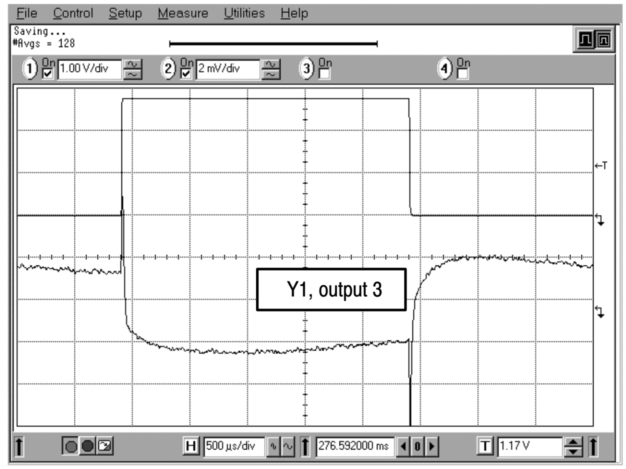


Figure 20. Vin = 5V, Y1 = 1mV/div

TECHNICAL TERMS

Rise Time − Common Enable being in ON state, the device is switched on by ON/OFF pin control.

Let's call t_1 the time when ON/OFF signal reaches 1% of its nominal value.

Let's call t_2 the time when output signal reaches 99% of its nominal value.

The rise time for this device is specified as:

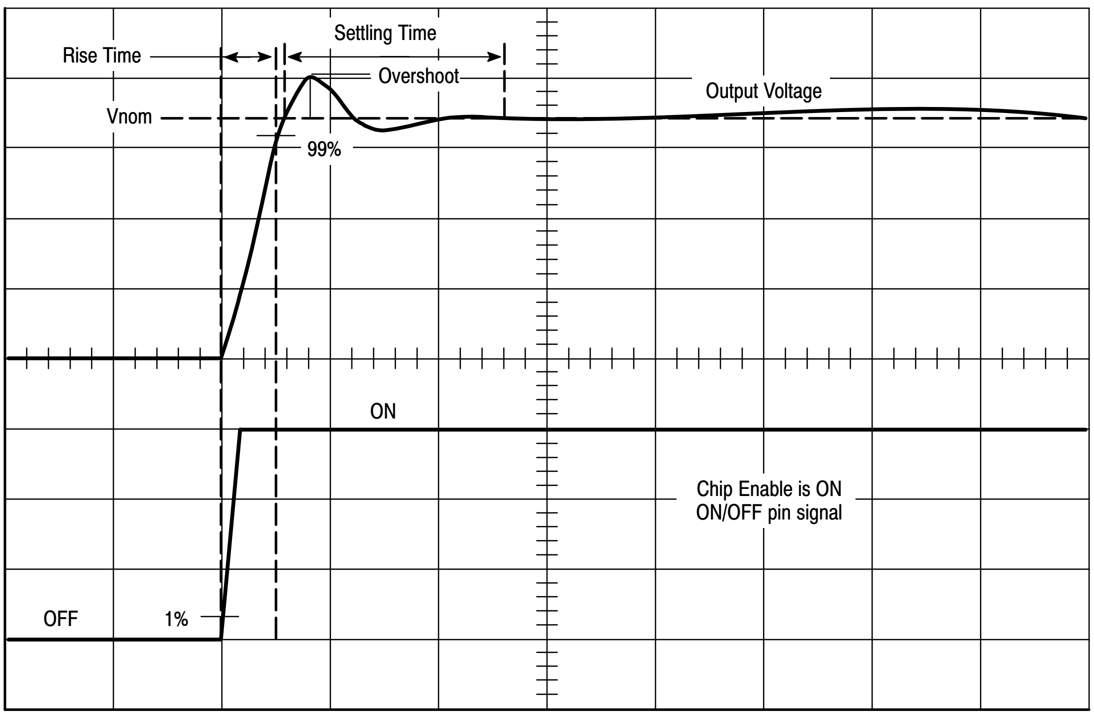
$$t_{ON} = t_1 - t_2$$

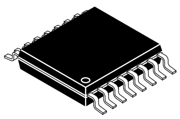
Fall Time − The fall time is highly dependent on the output capacitor and so device design is not impacting at all this parameter.

Overshoot, Settling Time − As regulators are based on regulation loop through an error amplifier, this type of device requires a certain time to stabilize and reach its nominal value.

The overshoot is defined as the voltage difference between the peak voltage and steady state when switching ON the regulator.

The settling time is equal to the time required by the regulator to stabilize to its nominal value (±0.5%) after peak value when switching ON the regulator.

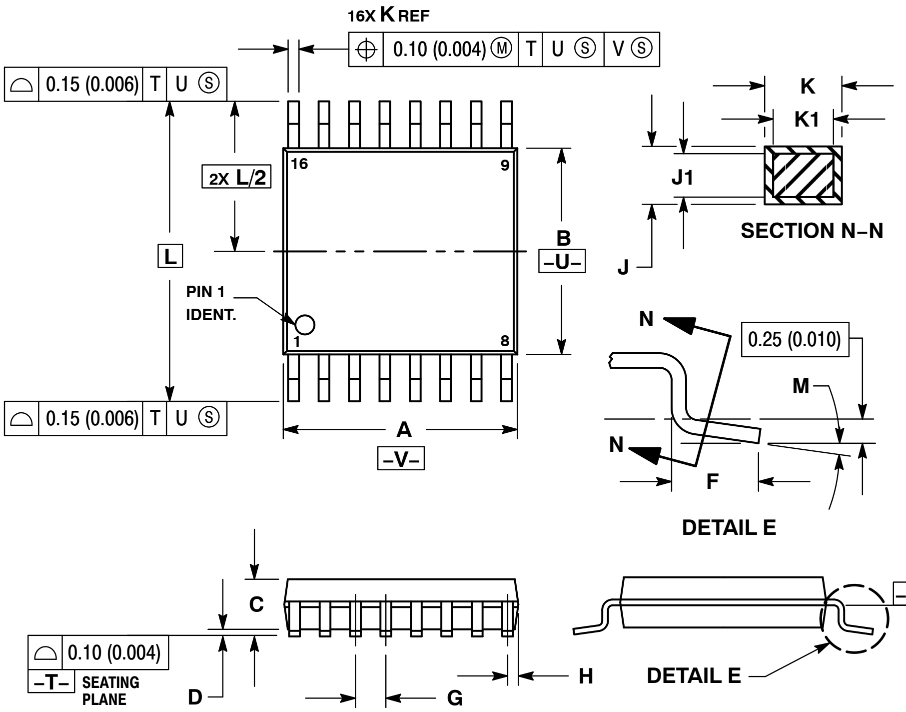




SCALE 2:1

TSSOP−16
CASE 948F−01
ISSUE B

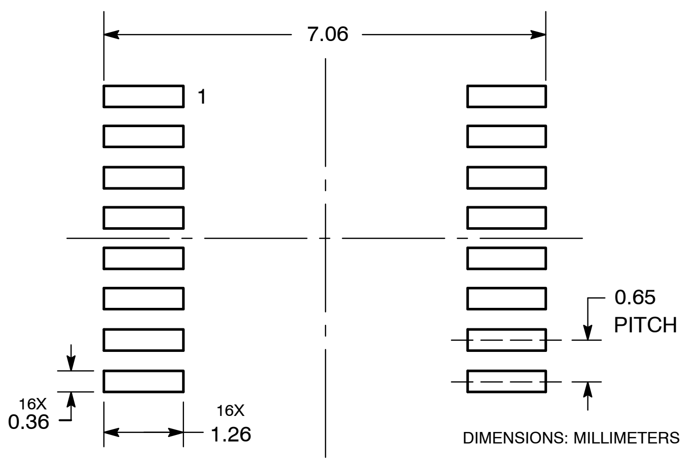
DATE 19 OCT 2006



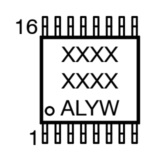
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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