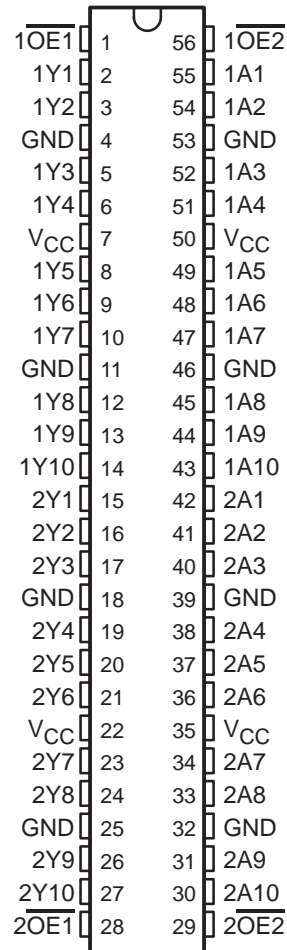


# SN54ABT16827, SN74ABT16827 20-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS220C – JUNE 1992 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art *EPIC-II B*™ BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16827 . . . WD PACKAGE  
SN74ABT16827 . . . DL PACKAGE  
(TOP VIEW)



## description

The 'ABT16827 are noninverting 20-bit buffers composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ( $\overline{1OE1}$  and  $\overline{1OE2}$  or  $\overline{2OE1}$  and  $\overline{2OE2}$ ) inputs must both be low for the corresponding Y outputs to be active. If either output-enable input is high, the outputs of that 10-bit buffer section are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16827 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT16827 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .



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 **TEXAS  
INSTRUMENTS**

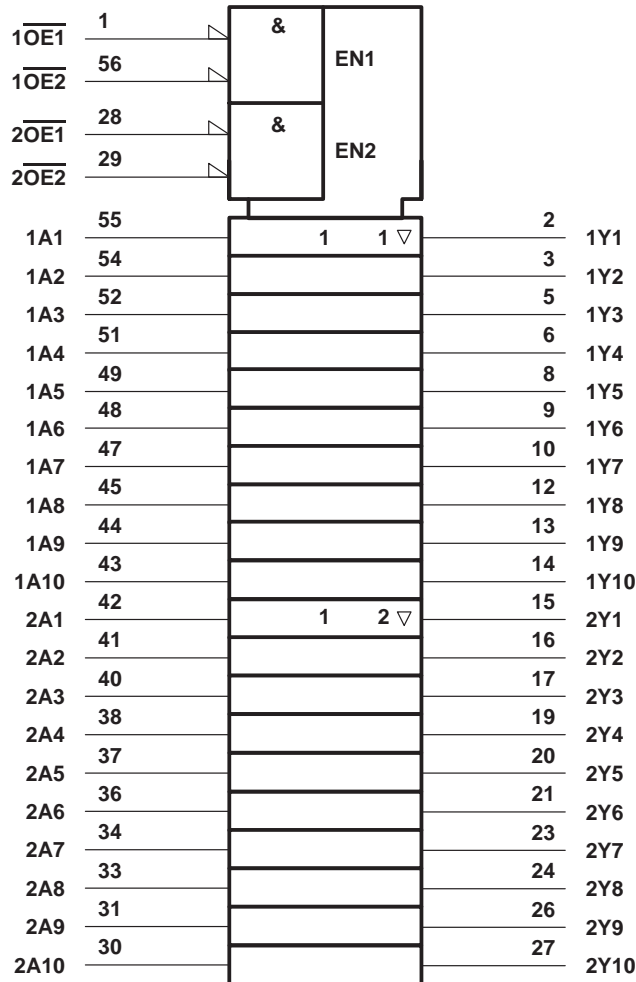
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FUNCTION TABLE  
(each 10-bit section)

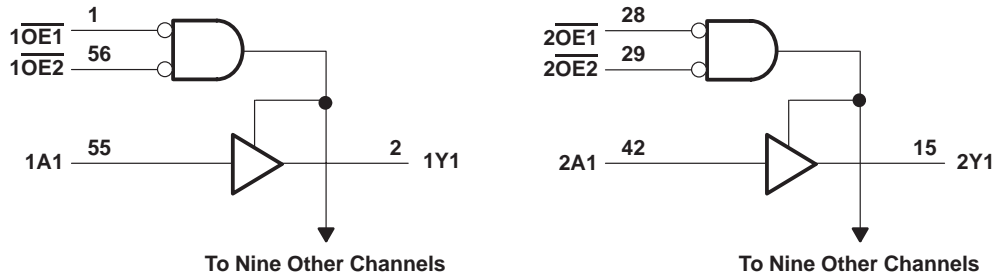
| INPUTS |     |   | OUTPUT |
|--------|-----|---|--------|
| OE1    | OE2 | A | Y      |
| L      | L   | L | L      |
| L      | L   | H | H      |
| H      | X   | X | Z      |
| X      | H   | X | Z      |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|   |                 |
|---|-----------------|
| Supply voltage range, $V_{CC}$ .....  | -0.5 V to 7 V   |
| Input voltage range, $V_I$ (see Note 1) .....                                   | -0.5 V to 7 V   |
| Voltage range applied to any output in the high or power-off state, $V_O$ ..... | -0.5 V to 5.5 V |
| Current into any output in the low state, $I_{O}$ : SN54ABT16827 .....          | 96 mA           |
| SN74ABT16827 .....  | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....                               | -18 mA          |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....                              | -50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DL package .....         | 74°C/W          |
| Storage temperature range, $T_{stg}$ .....                                      | -65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

|                          |                                    | SN54ABT16827 |          | SN74ABT16827 |          | UNIT      |
|--------------------------|------------------------------------|--------------|----------|--------------|----------|-----------|
|                          |                                    | MIN          | MAX      | MIN          | MAX      |           |
| $V_{CC}$                 | Supply voltage                     | 4.5          | 5.5      | 4.5          | 5.5      | V         |
| $V_{IH}$                 | High-level input voltage           | 2            |          | 2            |          | V         |
| $V_{IL}$                 | Low-level input voltage            |              | 0.8      |              | 0.8      | V         |
| $V_I$                    | Input voltage                      | 0            | $V_{CC}$ | 0            | $V_{CC}$ | V         |
| $I_{OH}$                 | High-level output current          |              | -24      |              | -32      | mA        |
| $I_{OL}$                 | Low-level output current           |              | 48       |              | 64       | mA        |
| $\Delta t/\Delta v$      | Input transition rise or fall rate | Control pins |          | 4            |          | ns/V      |
|                          |                                    | Data pins    |          | 10           |          |           |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate                 | 200          |          | 200          |          | $\mu s/V$ |
| $T_A$                    | Operating free-air temperature     | -55          | 125      | -40          | 85       | °C        |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

# SN54ABT16827, SN74ABT16827

## 20-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCBS220C – JUNE 1992 – REVISED MAY 1997

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                | TEST CONDITIONS  | T <sub>A</sub> = 25°C  |      |      | SN54ABT16827 |       | SN74ABT16827 |      | UNIT |    |
|--------------------------|--|--|------|------|--------------|-------|--------------|------|------|----|
|                          |  | MIN  | TYP† | MAX  | MIN          | MAX   | MIN          | MAX  |      |    |
| V <sub>IK</sub>          | V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA                                   |  |      | -1.2 |              | -1.2  |              | -1.2 | V    |    |
| V <sub>OH</sub>          | V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA                                   |  |      | 2.5  |              | 2.5   |              | 2.5  | V    |    |
|                          | V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA                                     |  |      | 3    |              | 3     |              | 3    |      |    |
|                          | V <sub>CC</sub> = 4.5 V  | I <sub>OH</sub> = -24 mA   |      |      | 2            |       | 2            |      |      | 2  |
| I <sub>OH</sub> = -32 mA |  |  |      | 2*   |              |       |              | 2    |      |    |
| V <sub>OL</sub>          | V <sub>CC</sub> = 4.5 V  | I <sub>OL</sub> = 48 mA  |      |      |              | 0.55  |              | 0.55 | V    |    |
|                          |  | I <sub>OL</sub> = 64 mA  |      |      |              | 0.55* |              | 0.55 |      |    |
| V <sub>hys</sub>         |  |  |      | 100  |              |       |              |      | mV   |    |
| I <sub>I</sub>           | V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND              |  |      | ±1   |              | ±1    |              | ±1   | µA   |    |
| I <sub>OZPU</sub> ‡      | V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$ |  |      | ±50  |              | ±50   |              | ±50  | µA   |    |
| I <sub>OZPD</sub> ‡      | V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$ |  |      | ±50  |              | ±50   |              | ±50  | µA   |    |
| I <sub>OZH</sub>         | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 2.7 V, $\overline{OE} \geq 2$ V |  |      | 10   |              | 10    |              | 10   | µA   |    |
| I <sub>OZL</sub>         | V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>O</sub> = 0.5 V, $\overline{OE} \geq 2$ V |  |      | -10  |              | -10   |              | -10  | µA   |    |
| I <sub>off</sub>         | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V                      |  |      | ±100 |              |       |              | ±100 | µA   |    |
| I <sub>CEX</sub>         | Outputs high   | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V                                      |      |      |              | 50    |              | 50   | µA   |    |
| I <sub>O</sub> §         |  | V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V                                      | -50  | -100 | -180         | -50   | -180         | -50  | -180 | mA |
| I <sub>CC</sub>          | Outputs high   | V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND |      |      |              | 2     |              | 2    | mA   |    |
|                          | Outputs low  |  |      |      |              | 32    |              | 32   |      |    |
|                          | Outputs disabled   |  |      |      |              | 2     |              | 2    |      |    |
| ΔI <sub>CC</sub> ¶       |  | V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND  |      |      |              | 1.5   |              | 1.5  | mA   |    |
| C <sub>i</sub>           |  | V <sub>I</sub> = 2.5 V or 0.5 V  |      |      |              | 3     |              |      | pF   |    |
| C <sub>o</sub>           |  | V <sub>O</sub> = 2.5 V or 0.5 V  |      |      |              | 7.5   |              |      | pF   |    |

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

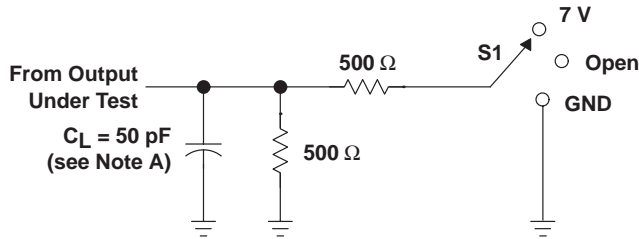
| PARAMETER        | FROM (INPUT)    | TO (OUTPUT) | V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C |     |     | SN54ABT16827 |     | SN74ABT16827 |     | UNIT |
|------------------|-----------------|-------------|--|-----|-----|--------------|-----|--------------|-----|------|
|                  |                 |             | MIN  | TYP | MAX | MIN          | MAX | MIN          | MAX |      |
| t <sub>PLH</sub> | A               | Y           | 1  | 1.9 | 3.1 | 1            | 3.6 | 1            | 3.4 | ns   |
| t <sub>PHL</sub> |                 |             | 1  | 2.1 | 3.7 | 1            | 4.5 | 1            | 4.2 |      |
| t <sub>PZH</sub> | $\overline{OE}$ | Y           | 1  | 2.8 | 5   | 1            | 5.9 | 1            | 5.6 | ns   |
| t <sub>PZL</sub> |                 |             | 1  | 2.8 | 4.9 | 1            | 5.8 | 1            | 5.5 |      |
| t <sub>PHZ</sub> | $\overline{OE}$ | Y           | 2.4  | 4.5 | 6.5 | 2.4          | 6.8 | 2.4          | 6.6 | ns   |
| t <sub>PLZ</sub> |                 |             | 1.6  | 3.7 | 5.7 | 1.6          | 7.1 | 1.6          | 6.1 |      |

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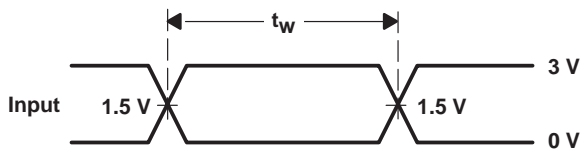
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PARAMETER MEASUREMENT INFORMATION

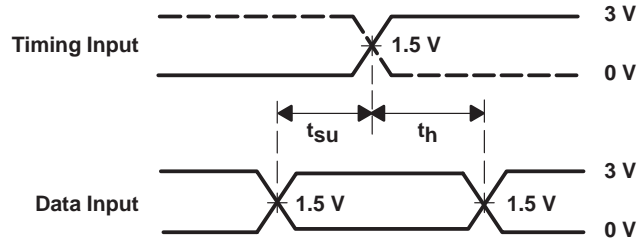


LOAD CIRCUIT

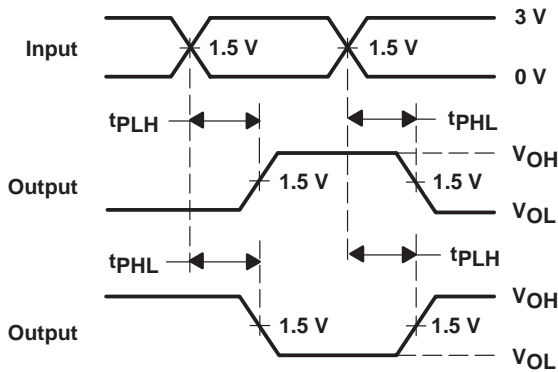
| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



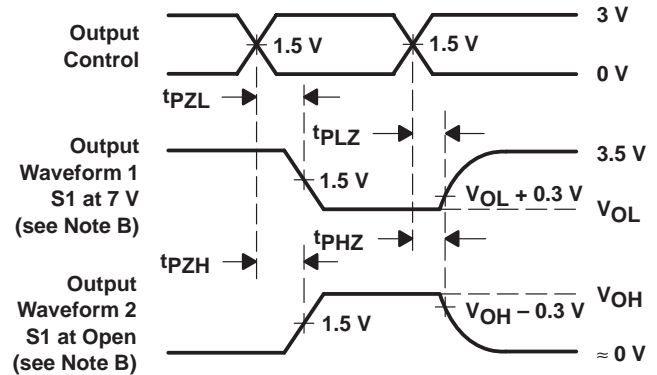
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74ABT16827DL   | ACTIVE        | SSOP         | DL              | 56   | 20          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT16827                | <a href="#">Samples</a> |
| SN74ABT16827DLG4 | ACTIVE        | SSOP         | DL              | 56   | 20          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT16827                | <a href="#">Samples</a> |
| SN74ABT16827DLR  | ACTIVE        | SSOP         | DL              | 56   | 1000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | ABT16827                | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16827DLR | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |



TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT16827DLR | SSOP         | DL              | 56   | 1000 | 367.0       | 367.0      | 55.0        |



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