Freescale Semiconductor, Inc.
Product Brief

Document Number: KL1XPB
Rev. 1, 04/2015

Kinetis KL1x – General-Purpose Ultra-Low-Power MCUs

Up to 256 KB Flash and 32 KB SRAM

1. Kinetis L family introduction

Kinetis L series microcontrollers (MCUs) combine the exceptional low-power performance with energy efficiency and ease of use of the new ARM® Cortex®-M0+ processor with the performance, peripheral sets, enablement, and scalability of the Kinetis 32-bit MCU portfolio.

The Kinetis ultra-low-power L series frees power-critical designs from 8- and 16-bit MCU limitations by combining excellent dynamic and stop currents with superior processing performance, a broad selection of on-chip Flash memory densities, and extensive analog, connectivity, and HMI peripheral options.

Kinetis ultra-low-power L series MCUs are also hardware- and software-compatible with the ARM Cortex-M4-based Kinetis K series, providing a scalable migration path for higher performance, memory, and feature integration.

Contents

2. Kinetis KL1x subfamily overview

The Kinetis KL1x is a general-purpose ultra-low-power MCU family, providing additional memory, communications, and analog peripheral options, beyond those offered in the Kinetis KL0x MCU family. The KL1x MCU family is also compatible with the Kinetis K10 MCU family (based on the ARM Cortex-M4 core) and with all other Kinetis KL2x, KL3x, and KL4x series MCU families, providing a migration path for higher performance and feature integration.

- KL13 – Provides up to 64KB flash and 8KB SRAM, built-in ROM boot-loader, enhanced mixed signal integration with high-accuracy VREF, ISO7816, two LPUARTs, FlexIO, and high-accuracy 48 MHz IRC
- KL14 – Broad offering with mixed signal integration, connectivity, and ultra-low power
- KL15 – Expansion from the KL14 family with the addition of 16-bit ADC and TSI
- KL16 – Expansion from the KL15 with up to 256 KB Flash and 32 KB SRAM, with the addition of I2S and 16-bit SPI
- KL17 – Latest member of KL1x, with up to 1:4 SRAM-to-Flash ratio, built-in ROM boot-loader, enhanced mixed signal integration with high-accuracy VREF, ISO7816, two LPUARTs, FlexIO, and high-accuracy 48 MHz IRC

3. Kinetis KL1x family key features

- Ultra-low-power 48 MHz devices supported with base line functions, up to 256 KB of Flash, and 32 KB of RAM.
- The asynchronous DMA allows for energy-saving peripherals; for example, ADC, UART, and Timer / PWM, to trigger asynchronous DMA request in the STOP / VLPS modes to perform DMA transfer and return to current power mode with no CPU intervention.
- The LPUART supports asynchronous transmit and receive operations to the bus clock, supporting communication down to the STOP / VLPS modes. Configurable receiver baud rate oversampling ratio from 4× to 32×, allowing for higher baud rates with lower clock sources.
- The SPI supports slave mode address match wakeup function and first message capture down to the STOP / VLPS modes.
- The I^2C supports multiple address match wakeup function down to the STOP / VLPS modes.
- The FlexIO is capable of emulating multiple serial interfaces, for example, UART, SPI, I^2C, IrDA, and is fully-functional under the STOP / VLPS modes.
- The LPTPM supports 16-bit timer input capture, output compare, and PWM functions, down to the STOP / VLPS modes.
- The LPTMR supports 16-bit timer and pulse counter functions in all power modes.
- The RTC supports 32-bit second counter with second interrupt and programmable alarm in all power modes with included temperature and voltage compensation.

- The ADC supports single conversions in multiple result registers down to the STOP / VLPS modes with hardware averaging and automatic compare modes.
- The CMP supports threshold crossing detection in all power modes (except VLLS0) along with a triggered compare mode for lower average power compares.
- The DAC and VREF support static reference in all power modes (except VLLS0).
- The TSI supports wake-on capacitive touch on single channel in all power modes.
- The LLWU supports eight wakeup pins, RESET and NMI wakeup pins, and energy-saving peripherals in the LLS and VLLSx modes.
- Outstanding low-power operation with core mark currents down to 100 µA / MHz, state retention stop mode down to 1.7 µA, with 7.5 µS wakeup time, and lowest power mode down to 87 nA.
- Highly reliable, fast-access Flash memory with four levels of protection for code security / protection.
- Faster time to market with comprehensive enablement solutions, including SDK (drivers, libraries, stacks), IDE, boot-loader, RTOS, online community, and more.

4. Kinetis KL1x family feature summary

Table 1. Family feature summary

Sub-Family	KL13	KL14	KL15	KL16	KL17
CPU Frequency	48MHz	48MHz	48MHz	48MHz	48MHz
Flash Memory	32-64KB	32-64KB	32-128KB	32-256KB	32-256KB
SRAM	4-8KB	4-8KB	4-16KB	4-32KB	8-32KB
ROM Bootloader	Yes	-	-	-	Yes
Analog	16bit ADC, 12bit DAC, CMP, VREF	12bit ADC, CMP	16bit ADC, 12bit DAC, CMP	16bit ADC, 12bit DAC, CMP	16bit ADC, 12bit DAC, CMP, VREF
Connectivity	UART w/ ISO7816, LPUART, SPI, I2C, FlexIO	UART, LPUART, SPI, I2C	UART,LPUART, SPI, I2C	UART,LPUART, SPI, I2C I2S	UART w/ ISO7816,LPUART, SPI, I2C, I2S, FlexIO
Package Options	32QFN, 48QFN, 64LQFP, 64MAPBGA, 80LQFP	32QFN, 48QFN, 64LQFP, 80LQFP	32QFN, 35WLCSP, 48QFN, 64LQFP,80LQFP	32QFN, 48QFN, 64LQFP, 64MAPBGA	32QFN, 48QFN, 36XFBGA, 64LQFP, 64MAPBGA

5. Kinetis KL1x family block diagram

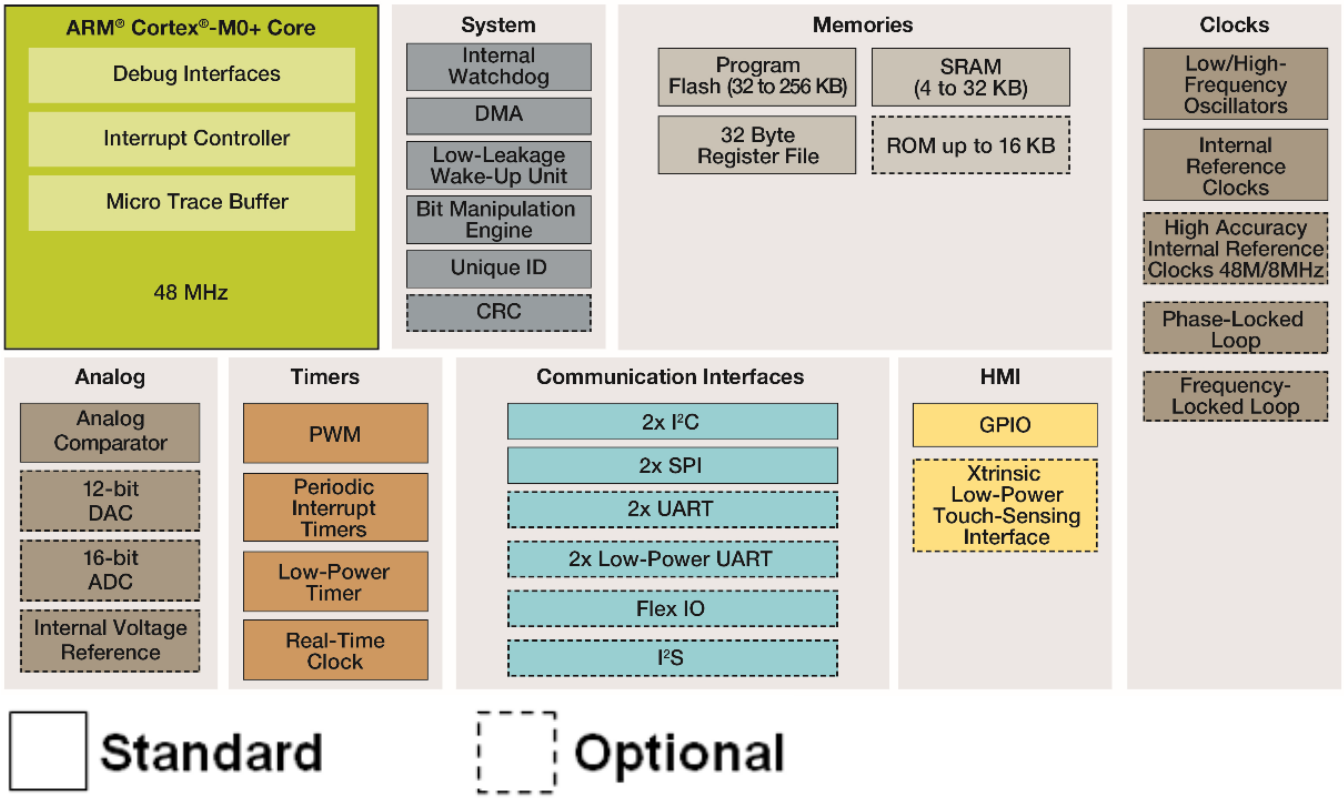

Figure 1. Kinetis KL1x family block diagram

6. KL1x family common features

The following features are present on all KL1x MCUs:

- 48 MHz Cortex-CM0+
- 2-pin serial wire debug (SWD), micro trace buffer (MTB)
- 4-channel DMA controller
- Integrated bit manipulation engine (BME)
- 64-Byte cache and 32-Byte register file
- 1 ×6-channel and 2 ×2-channel LPTPM
- Low- and high-frequency OSC
- RTC (32 KHz OSC)
- 1 ×low-power timer, 1 ×2-channel PIT
- High-speed analog comparator containing a 6-bit DAC for programmable reference input

- Power management controller (PMC) with nine power modes
- Non-maskable interrupt (NMI)
- Software and COP watchdog
- 80-bit unique identification number per chip
- Voltage range 1.71 V – 3.6 V
- Temperature range (TA) -40°C – 105°C

7. Kinetis KL1x family differences

Table 2. Family differences

Sub-Family		KL13	KL14	KL15	KL16	KL17
CPU Frequency		48MHz	48MHz	48MHz	48MHz	48MHz
Memory	Flash/SRAM Size	32KB/4KB - 64KB/8KB	32KB/4KB - 128KB/16KB	32KB/4KB - 128KB/16KB	32KB/4KB - 256KB/32KB	32KB/8KB - 128KB/32KB, 256KB/32KB
	Boot ROM	8KB	-	-	-	16KB
Communication Interface	LPUART	2	1	1	1	2
	UART	1	2	2	2	-
	UART w/ ISO7816	1	-	-	-	1
	SPI	2[2]	2[1]	2[1]	2[2]	2[2]
	I2C	2[3]	2	2	2	2[3]
	I2S	-	-	-	1	1
	FlexIO	YES	-	-	-	YES
Analog Modules	ADC	16-bit	12-bit	16-bit	16-bit	16-bit
	ADC Channels (SE/DE)	11/2 - 20/4	11/0 - 20/0	11/2 - 20/4	11/2 - 20/4	11/2 - 20/4
	DAC	12-bit	-	12-bit	12-bit	Optional[4]
	VREF	Optional[6]	-	-	-	YES
Other Modules	CRC	YES	-	-	-	Optional[5]
	TSI	-	-	9ch - 16ch	9ch - 16ch	-
	Total GPIOs	28 - 70	28 - 70	28 - 70	28 - 54	28 - 54
	MCG	High Accuracy 48MHz IRC, 8/2MHz IRC	4MHz/32KHz IRC PLL/FLL	4MHz/32KHz IRC PLL/FLL	4MHz/32KHz IRC PLL/FLL	High Accuracy 48MHz IRC, 8/2MHz IRC

Sub-Family	KL13	KL14	KL15	KL16	KL17
Package Options	32QFN, 48QFN, 64LQFP, 64MAPBGA, 80LQFP	32QFN, 48QFN, 64LQFP, 80LQFP	32QFN, 35WLCSP, 48QFN, 64LQFP, 80LQFP	32QFN, 48QFN, 64LQFP, 64MAPBGA	32QFN, 48QFN, 64LQFP, 64MAPBGA, 36XFBGA

[1] 8-bit SPI, one SPI with FiFo
[2] 16-bit SPI, one SPI with FiFo
[3] Double buffering with support up to 1 Mbps
[4] DAC is only available in 128 KB and 256 KB Flash KL17
[5] CRC is only available in 32 KB and 64 KB Flash KL17
[6] VREF is not available in 32QFN

8. Comprehensive enablement solutions

8.1. Kinetis Software Development Kit (SDK)

- Extensive suite of robust peripheral drivers, stacks, and middleware.
- Includes software examples demonstrating the usage of HAL, peripheral drivers, middleware, and RTOSes.
- Operating system abstraction (OSA) for Freescale MQX™ Lite RTOS, FreeRTOS, and Micrium uC / OS kernels and bare-metal (no RTOS) applications.

8.2. Processor Expert

- Free software generation tool for device drivers / start-up code
- Seven steps from project creation to debug – dramatically reduces development time
- Available within Kinetis Design Studio or as a standalone plug-in for IAR/Keil/GNU IDEs

8.3. Integrated development environments (IDE)

- Atollic® TrueSTUDIO® atollic.com/index.php/partnerfreescale
- Green Hills Software MULTI ghs.com/products/kinetis.html
- IAR Embedded Workbench® iar.com/kinetis
- ARM Keil® Microcontroller Development Kit keil.com/freescale
- Freescale Kinetis Design Studio IDE
  - No-cost integrated development environment (IDE) for Kinetis MCUs
  - Eclipse and GCC-based IDE for C / C++ editing, compiling, and debugging

- Broad ARM ecosystem support through Freescale Connect partners

8.4. Online enablement with ARM mbed™ development platform

- Rapid and easy Kinetis MCU prototyping and development
- Online mbed SDK, developer community
- Free software libraries

8.5. Freescale MQX™ Lite RTOS

- Free, light-weight MQX kernel customised for small resource MCUs
- Packaged as a Processor Expert component
- Upwards compatible with MQX RTOS

8.6. Boot-loader

- Common boot-loader for all Kinetis MCUs
- In-system Flash programming over a serial connection: erase, program, verify
- ROM- or Flash-based boot-loader with open-source software and host-side programming utilities

8.7. Development hardware

- Tower System modular development platform
  - Modular and Expandable
  - Rapid prototyping and evaluation
  - Cost Effective
- Freescale Freedom development platforms
  - Low cost (< $ 20 USD)
  - Designed in an industry-standard compact form factor
  - Integrated open-standard serial and debug interface (OpenSDA)
  - Compatible with a rich-set of third-party expansion boards

9. Part identification

9.1. Description

The chip part numbers have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

9.2. Format

The device part numbers have the following format: Q KL## A FFF T PP CC (N)

9.3. Fields

The following table lists the possible values for each field in the part number (not all combinations are valid).

Table 3. Part number field descriptions

Field	Description	Values
Q	Qualification status	M = Fully-qualified, general market flow P = Prequalification
KL##	Kinetis family	KL13 KL14 KL15 KL16 KL17
A	Key attribute	Z = Cortex-M0+
FFF	Program Flash memory size	32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB
R	Silicon revision	(Blank) = Main A = Revision after main
T	Temperature range	V = -40ºC – 105ºC
PP	Package identifier	FM = 32QFN (5 mm × 5 mm × 0.65 mm, Pitch 0.5mm) AD = 35WLCSP (2.5 mm × 3 mm × 0.6mm, Pitch 0.4mm) DA = 36XFBGA (3.5 mm × 3.5 mm × 0.5mm, Pitch 0.65mm) FT = 48QFN (7 mm × 7 mm × 0.65mm, Pitch 0.5mm) LH = 64LQFP (10 mm × 10 mm × 1.4mm, Pitch 0.5mm) MP = 64MAPBGA (5 mm × 5 mm × 1.5mm, Pitch 0.5mm) LK = 80LQFP (12 mm × 12 mm × 1.6mm, Pitch 0.5mm)
CC	Maximum CPU frequency (MHz)	4 = 48 MHz

Table 3. Part number field descriptions

Field	Description	Values
N	Packaging type	R = Tape and reel (Blank) = Trays

10. Orderable part numbers

Table 4. Ordering information

Product	Memory		Package		IO and ADC Channel		
MC Partnumber	Flash (KB)	SRAM (KB)	Pin Count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC Channels (SE/DP)
MKL13Z32VFM4	32	4	32	QFN[2]	28	28/4	11/2
MKL13Z32VFT4	32	4	48	QFN[2]	40	40/4	18/2
MKL13Z32VLH4	32	4	64	LQFP	54	54/4	20/4
MKL13Z32VMP4	32	4	64	MAPBGA[2]	54	54/4	20/4
MKL13Z32VLK4	32	4	80	LQFP	70	70/4	20/4
MKL13Z64VFM4	64	8	32	QFN[2]	28	28/4	11/2
MKL13Z64VFT4	64	8	48	QFN[2]	40	40/4	18/2
MKL13Z64VLH4	64	8	64	LQFP	54	54/4	20/4
MKL13Z64VMP4	64	8	64	MAPBGA[2]	54	54/4	20/4
MKL13Z64VLK4	64	8	80	LQFP	70	70/4	20/4
MKL14Z32VFM4	32	4	32	QFN	28	19/4	11/0
MKL14Z64VFM4	64	8	32	QFN	28	19/4	11/0
MKL14Z32VFT4	32	4	48	QFN	40	24/4	18/0
MKL14Z64VFT4	64	8	48	QFN	40	24/4	18/0
MKL14Z32VLH4	32	4	64	LQFP	54	31/4	20/0
MKL14Z64VLH4	64	8	64	LQFP	54	31/4	20/0
MKL14Z32VLK4	32	4	80	LQFP	70	39/4	20/0
MKL14Z64VLK4	64	8	80	LQFP	70	39/4	20/0
MKL15Z32VFM4	32	4	32	QFN	28	19/4	11/2
MKL15Z64VFM4	64	8	32	QFN	28	19/4	11/2
MKL15Z128VFM4	128	16	32	QFN	28	19/4	11/2
MKL15Z128CAD4	128	16	35	WLCSP	31	19/4	14/3
MKL15Z32VFT4	32	4	48	QFN	40	24/4	18/3
MKL15Z64VFT4	64	8	48	QFN	40	24/4	18/3
MKL15Z128VFT4	128	16	48	QFN	40	24/4	18/3
MKL15Z32VLH4	32	4	64	LQFP	54	31/4	20/4

Product	Memory		Package		IO and ADC Channel		
MC Partnumber	Flash (KB)	SRAM (KB)	Pin Count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC Channels (SE/DP)
MKL15Z64VLH4	64	8	64	LQFP	54	31/4	20/4
MKL15Z128VLH4	128	16	64	LQFP	54	31/4	20/4
MKL15Z32VLK4	32	4	80	LQFP	70	31/4	20/4
MKL15Z64VLK4	64	8	80	LQFP	70	31/4	20/4
MKL15Z128VLK4	128	16	80	LQFP	70	31/4	20/4
MKL16Z32VFM4	32	4	32	QFN	28	19/4	11/2
MKL16Z64VFM4	64	8	32	QFN	28	19/4	11/2
MKL16Z128VFM4	128	16	32	QFN	28	19/4	11/2
MKL16Z32VFT4	32	4	48	QFN	40	24/4	18/3
MKL16Z64VFT4	64	8	48	QFN	40	24/4	18/3
MKL16Z128VFT4	128	16	48	QFN	40	24/4	18/3
MKL16Z32VLH4	32	4	64	LQFP	54	31/4	20/4
MKL16Z64VLH4	64	8	64	LQFP	54	31/4	20/4
MKL16Z128VLH4	128	16	64	LQFP	54	31/4	20/4
MKL16Z256VLH4	256	32	64	LQFP	54	31/4	20/4
MKL16Z256VMP4	256	32	64	MAPBGA	54	31/4	20/4
MKL17Z32VFM4	32	8	32	QFN[2]	28	28/6	11/2
MKL17Z64VFM4	64	16	32	QFN[2]	28	28/6	11/2
MKL17Z32VDA4	32	8	36	XFBGA	32	32/6	15/4
MKL17Z64VDA4	64	16	36	XFBGA	32	32/6	15/4
MKL17Z32VFT4	32	8	48	QFN[2]	40	40/6	18/3
MKL17Z64VFT4	64	16	48	QFN[2]	40	40/6	18/3
MKL17Z32VMP4	32	8	64	MAPBGA[2]	54	54/6	20/4
MKL17Z64VMP4	64	16	64	MAPBGA[2]	54	54/6	20/4
MKL17Z32VLH4	32	8	64	LQFP	54	54/6	20/4
MKL17Z64VLH4	64	16	64	LQFP	54	54/6	20/4
MKL17Z128VFM4	128	32	32	QFN	28	19/6	11/2
MKL17Z256VFM4	256	32	32	QFN	28	19/6	11/2
MKL17Z128VFT4	128	32	48	QFN	40	24/6	18/3
MKL17Z256VFT4	256	32	48	QFN	40	24/6	18/3
MKL17Z128VLH4	128	32	64	LQFP	54	31/6	20/4
MKL17Z256VLH4	256	32	64	LQFP	54	31/6	20/4
MKL17Z128VMP4	128	32	64	MAPBGA	54	31/6	20/4

Product	Memory		Package		IO and ADC Channel		
MC Partnumber	Flash (KB)	SRAM (KB)	Pin Count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC Channels (SE/DP)
MKL17Z256VMP4	256	32	64	MAPBGA	54	31/6	20/4

[1] INT: interrupt pin numbers; HD: high drive pin numbers
[2] This package is included in a Package Your Way program for Kinetis MCUs. Please visit Freescale.com/KPYW for more detail.

Table 5. Revision history

Revision	Substantial changes
0	Initial release
1	Update with KL13 information

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Document Number: KL1XPB
Rev. 1
04/2015