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REFERENCE DESIGN 4195 INCLUDES: √Tested Circuit √Schematic √Description √Test Data √Software

Selecting SPI Clock Modes for Interfacing the MAX1132 ADC with the MAXQ2000 Microcontroller

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Abstract: The MAXQ2000 can interface with the MAX1132 using different clock modes: 8-bit, 16-bit, or a combination of both. This application note describes how to select an SPI™ clock mode that will optimize the performance of the MAX1132. Included in the application note are complete schematics and microcontroller firmware, as well as an example C program that was written and assembled for the IAR Embedded Workbench® for MAXQ®.

Note: The suffix "-bar" (CS-bar) indicates the active-low functionality of the CS pin.

MAX1132 Overview

The MAX1132 is a 200ksps, 16-bit ADC. The MAXQ2000 can interface with the MAX1132 in a variety of SPI clock modes: 8-bit, 16-bit, or a combination of both. To maximize the performance of the ADC, it is important to determine which mode to use during early stages of development. It is obvious that a 16-bit ADC with 16 clock frames should use 16-bit mode; however, in a scenario where the ADC uses 24 clock frames, the SPI clock mode must be evaluated closely. This application note provides test results for 8-bit mode, 16-bit mode, and combination mode; the results indicate that combination mode is optimal when the MAX1132 uses 24 clock frames.

Hardware Overview

This application circuit utilizes the MAX1132EVKIT and MAXQ2000-KIT.

Figure 1 presents the MAX1132 EV kit schematic, and **Figure 2** illustrates the configuration of the system. To interface the MAX1132 EV kit with the MAXQ2000-KIT, connect SCLK, CS-bar, DOUT, and DIN from the MAX1132 EV kit to the MAXQ2000-KIT, as shown in Figure 2. In addition, a +5V supply is applied on the AV$_{DD}$ and AGND terminals of the EV kit. JU1 of the EV kit must be installed on 1–2 (ON) position. Apply an analog signal up to +12V on JU2, and the rest of the jumpers are left open. SW3 of the MAXQ2000-KIT must be turned off for proper operation of the system.
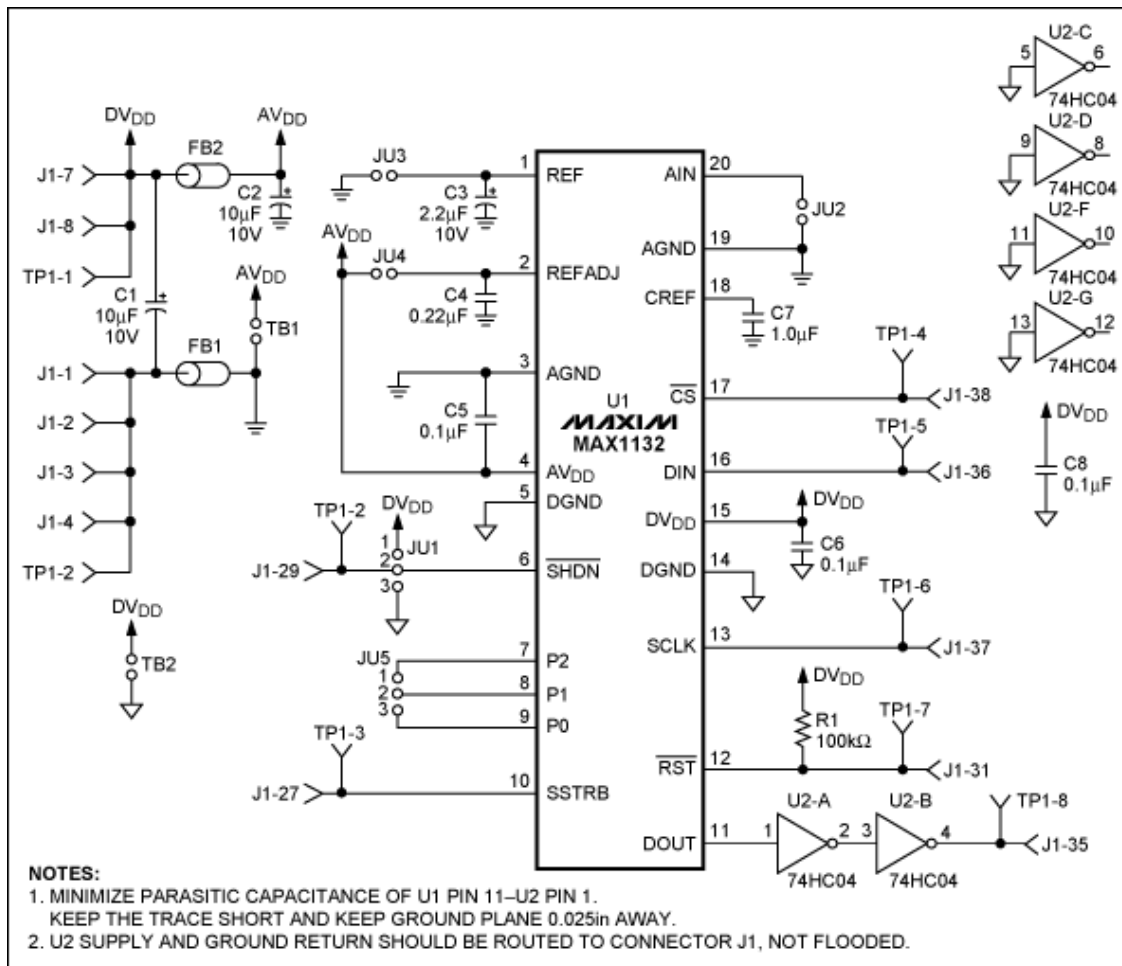
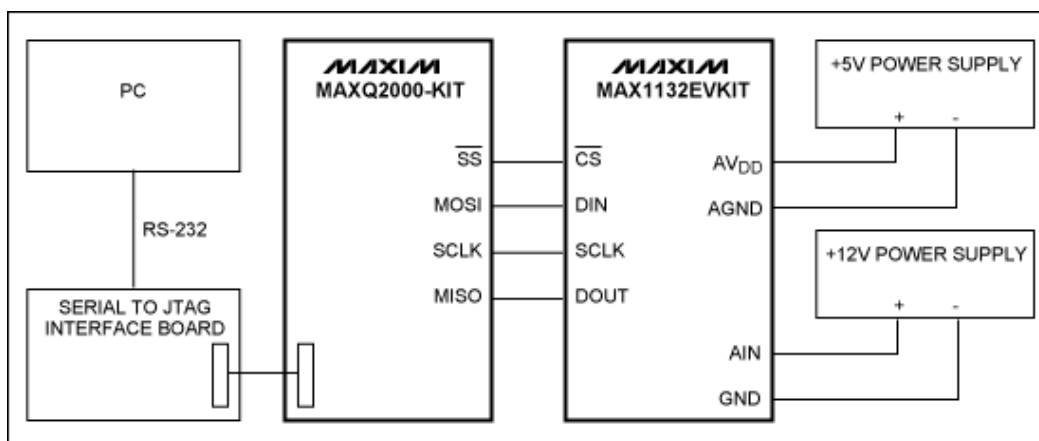Figure 1. The schematic for the MAX1132 EV kit.

Figure 2. The system block diagram of the hardware used to evaluate the different SPI clock modes.

Analysis

The simplest and most flexible SPI clock mode is 8-bit mode because three bytes fit perfectly into 24 clock frames, and the MAX1132 needs 24 clock frames to complete a data transfer. The most significant byte is used as the control byte (0x80), which is sent to the slave. The most significant bit is crucial because it flags

the slave to start the conversion (refer to the MAX1132 datasheet for the control byte format). The two least significant bytes are the data received from the ADC. Ideally, with the MAXQ2000's SPI serial clock running at 4MHz, the ADC should be able to maximize the sampling rate at approximately 166.67ksps. **Table 1** shows the oscilloscope channel designated to each signal connected to the ADC.

Table 1. Oscilloscope Channel Assignment

Channel	Signal
1	CS-bar
2	SCLK
3	DIN
4	DOUT

The sample rate of the MAX1132 in 8-bit mode is approximately 63.7ksps. The sample rate is slower than expected because the serial clock includes the following delays: CS-bar goes low when SCLK goes high; one set of clocks transitions to the next set of clocks; SCLK goes low when CS-bar goes high; and CS-bar stays high before another sample starts (**Figure 3**).
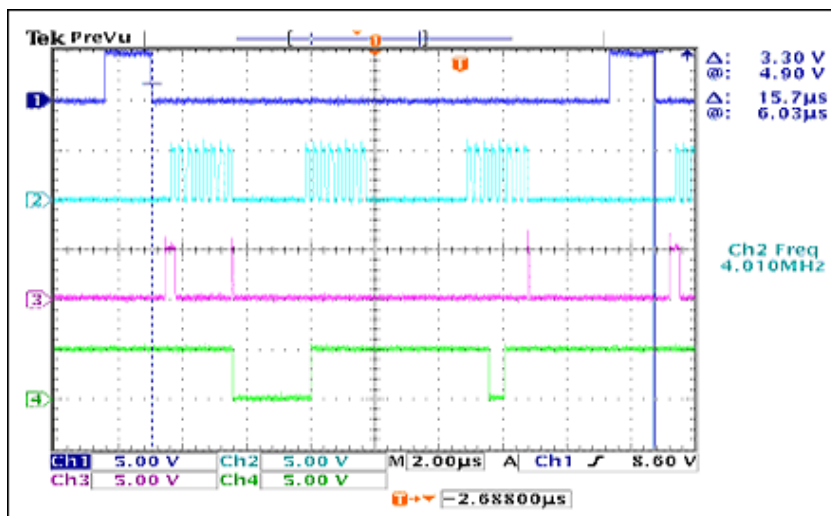

Figure 3. A sample from a block of samples in 8-bit mode.

When the SPI clock is in 16-bit mode, two sets of 16 clocks (32 clocks total) are needed. The most significant byte of the first 16 clocks is the control byte sent by the microcontroller, and the next byte is the most significant byte of the data received from the ADC. During the second 16 clocks, the least significant byte of the data is received from the ADC. The rest of the 8 clocks in the frame must be used for the same sample to be consistent when transferring consecutive data. **Figure 4** indicates that the sample rate is 63.7ksps, which is the same as 8-bit mode.
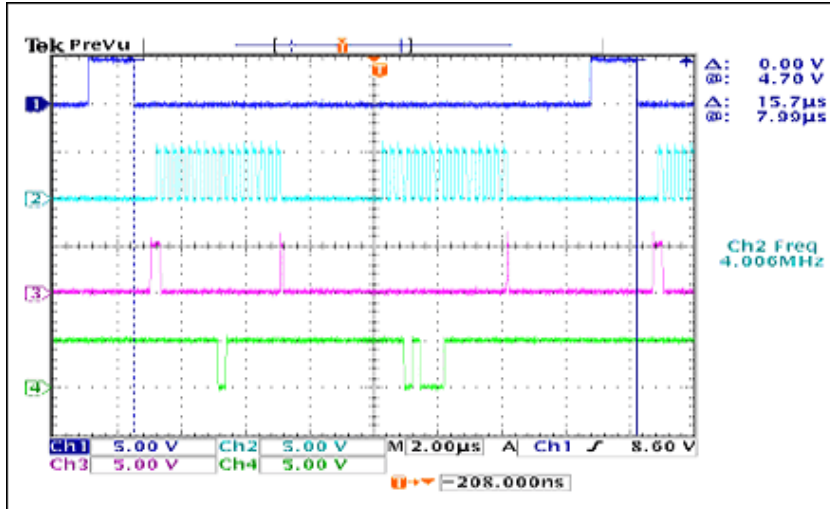
Figure 4. A sample from a block of samples in 16-bit mode.

A better option is to first use the 8-bit SPI clock mode to send the control byte and, then, switch to 16-bit SPI clock mode to receive the sample from the ADC (**Figure 5**). The advantage here is that it does not separate the data received in different sets of clocks and does not waste any cycles. In combination mode, the sample rate is 70.4ksps, which is faster than both 8-bit mode and 16-bit mode.
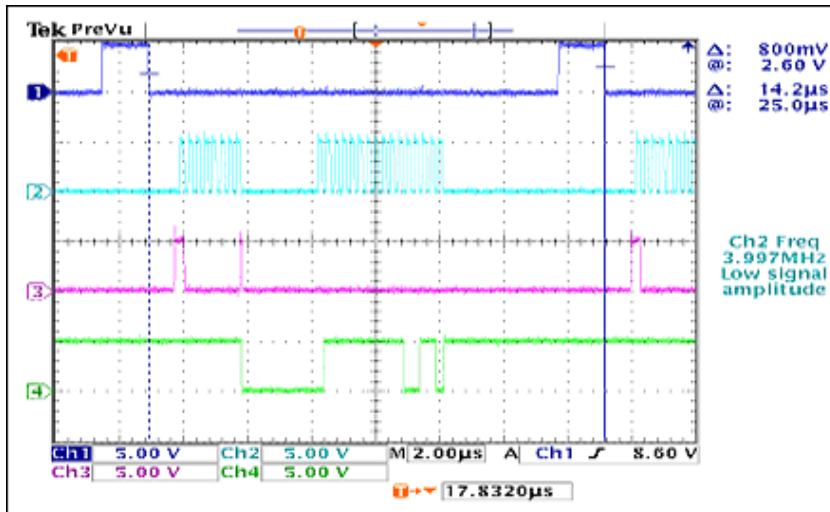

Figure 5. A sample from combination mode, which uses 8-bit mode to send the control byte, followed by 16-bit mode to receive the sample from the ADC.

The data collected from the samples above can be summarized with the time chart shown in **Table 2**. Combination mode is the ideal choice for optimizing the performance of the MAX1132. This mode uses a minimum set of clocks and a minimum amount of cycles within a frame. On their own, neither 8-bit mode nor 16-bit mode can achieve the speed of combination mode.

Table 2. Times at Different Intervals for a Single Sample

Interval	Sample Time, 8-Bit Mode	Sample Time, 16-Bit Mode	Sample Time, Combination Mode
CS-bar low to SCLK high	560ns	760ns	960ns
Between 1st and 2nd clock sets	2.32µs	3.20µs	2.36µs

Between 2nd and 3rd clock sets	3.12µs	—	—
SCLK low to CS-bar high	2.52µs	2.60µs	3.60µs
CS-bar high	1.48µs	1.44µs	1.48µs
Clock time (1/SCLK x clocks/frame)	6.0µs	8.0µs	6.0µs
Approximate total for one sample	15.7µs = 63.7ksps	15.7µs = 63.7ksps	14.2µs = 70.4ksps

Firmware Overview

The example C program files (written and assembled for the IAR Embedded Workbench for MAXQ) allow the MAXQ2000 SPI interface to communicate with the MAX1132 in combination mode. The SPI's serial clock is 4MHz when the system clock of the MAXQ2000 uses a 16MHz clock.

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Related Parts		
MAX1132	16-Bit ADC, 200ksps, 5V Single-Supply with Reference	Free Samples
MAXQ2000	Low-Power LCD Microcontroller	Free Samples

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