

MOSFET – N-Channel, DUAL COOL[®], POWERTRENCH[®]

120 V, 128 A, 4.2 mΩ

FDMT800120DC

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process. Advancements in both silicon and DUAL COOL package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

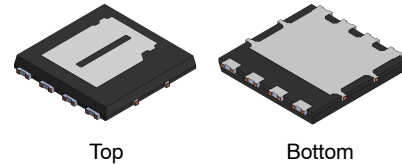
Features

- Max $r_{DS(on)}$ = 4.2 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$
- Max $r_{DS(on)}$ = 6.4 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 16\text{ A}$
- Advanced Package and Silicon Combination for Low $r_{DS(on)}$ and High Efficiency
- Next Generation Enhanced Body Diode Technology, Engineered for Soft Recovery
- Low Profile 8x8 mm MLP Package
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is RoHS Compliant

Typical Applications

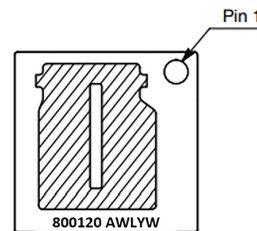
- OringFET/Load Switching
- Synchronous Rectification
- DC-DC Conversion

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
120 V	4.2 mΩ @ 10 V	128 A
	6.4 mΩ @ 6 V	



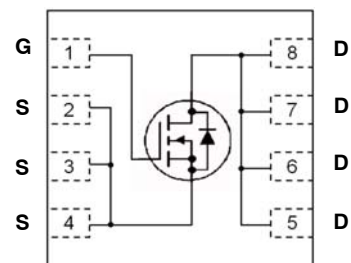
TDFNW8 8.3 x 8.4, 2P,
DUAL COOL, OPTION 2
CASE 507AR

MARKING DIAGRAM



800120 = Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

ELECTRICAL CONNECTION



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

FDMT800120DC

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
V_{DS}	Drain to Source Voltage	120	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current –Continuous $T_C = 25^\circ\text{C}$ (Note 5)	128	A
	–Continuous $T_C = 100^\circ\text{C}$ (Note 5)	81	
	–Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	20	
	–Pulsed (Note 4)	767	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	1350	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	156	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	1.6	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	9	

FDMT800120DC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	120	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	97	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 96 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–12	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 20 A	–	3.45	4.2	mΩ
		V _{GS} = 6 V, I _D = 16 A	–	4.6	6.4	
		V _{GS} = 10 V, I _D = 20 A, T _J = 125°C	–	6.3	7.7	
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 20 A	–	69	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 60 V, V _{GS} = 0 V, f = 1 MHz	–	5605	7850	pF
C _{oss}	Output Capacitance		–	778	1090	pF
C _{rss}	Reverse Transfer Capacitance		–	27	40	pF
R _g	Gate Resistance		0.1	1.4	3.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 60 V, I _D = 20 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	29	47	ns
t _r	Rise Time		–	18	33	
t _{d(off)}	Turn-Off Delay Time		–	40	64	
t _f	Fall Time		–	9.5	19	
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 60 V, I _D = 20 A	–	76	107	nC
		V _{GS} = 0 V to 6 V, V _{DD} = 60 V, I _D = 20 A	–	48	68	
Q _{gs}	Gate to Source Charge	V _{DD} = 60 V, I _D = 20 A	–	25	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	15	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.9 A (Note 2)	–	0.7	1.1	V
		V _{GS} = 0 V, I _S = 20 A (Note 2)	–	0.8	1.2	
t _{rr}	Reverse Recovery Time	I _F = 20 A, di/dt = 100 A/μs	–	87	139	ns
Q _{rr}	Reverse Recovery Charge		–	164	263	nC

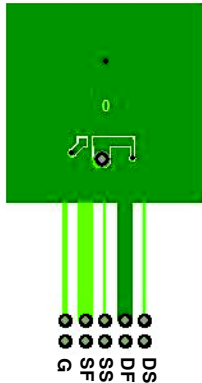
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	1.6	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	0.8	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	14	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	60	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	15	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	21	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	9	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	11	

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 81°C/W when mounted on a minimum pad of 2 oz copper.

- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- Still air, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- Still air, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- 200 FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- 200 FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- 200 FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- 200 FPM Airflow, 20.9 × 10.4 × 12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
- 200 FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- 200 FPM Airflow, 45.2 × 41.4 × 11.7 mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- E_{AS} of 1350 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3\text{ mH}$, $I_{AS} = 30\text{ A}$, $V_{DD} = 120\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 93\text{ A}$.
- Pulsed Id please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

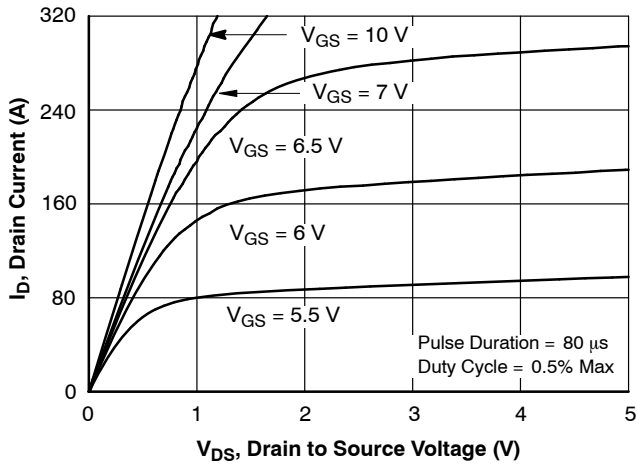


Figure 1. On Region Characteristics

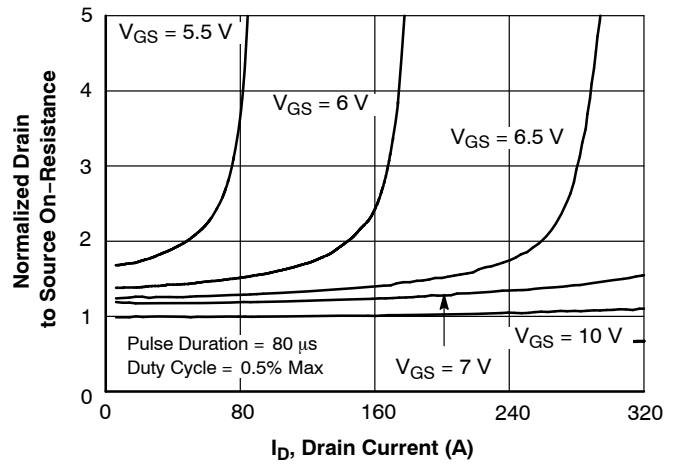


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

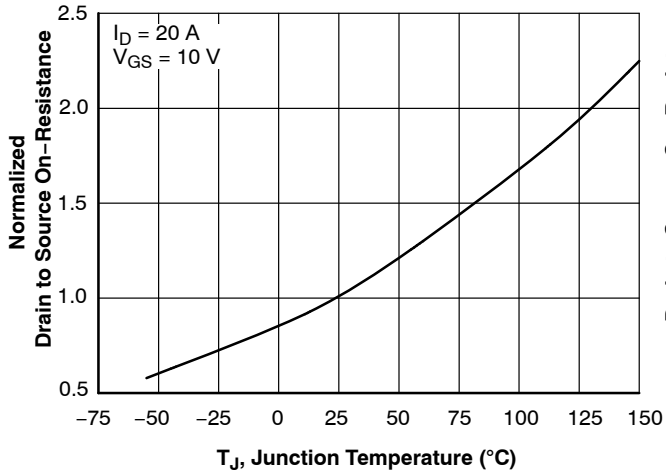


Figure 3. Normalized On Resistance vs. Junction Temperature

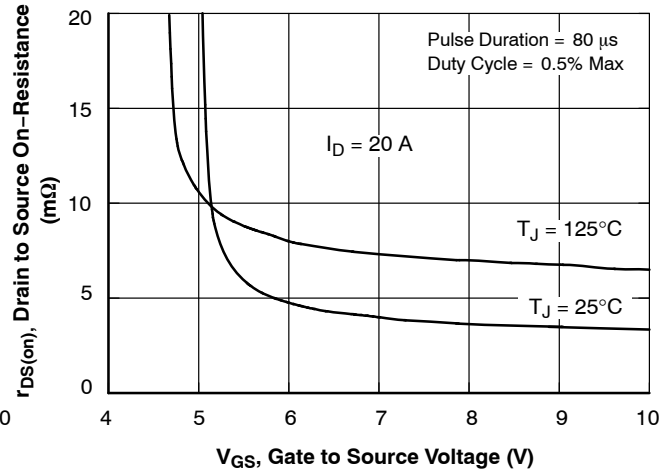


Figure 4. On-Resistance vs. Gate to Source Voltage

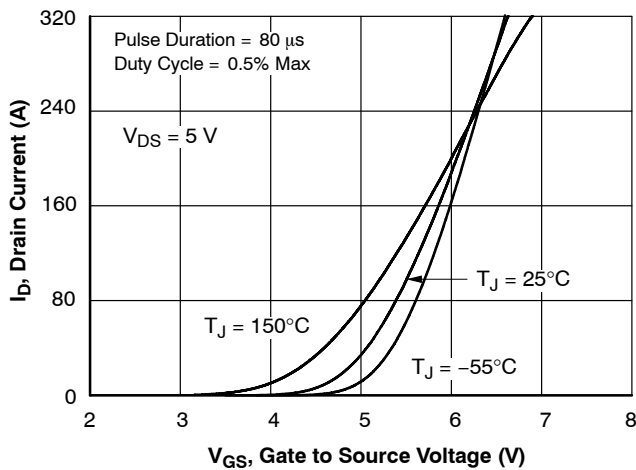


Figure 5. Transfer Characteristics

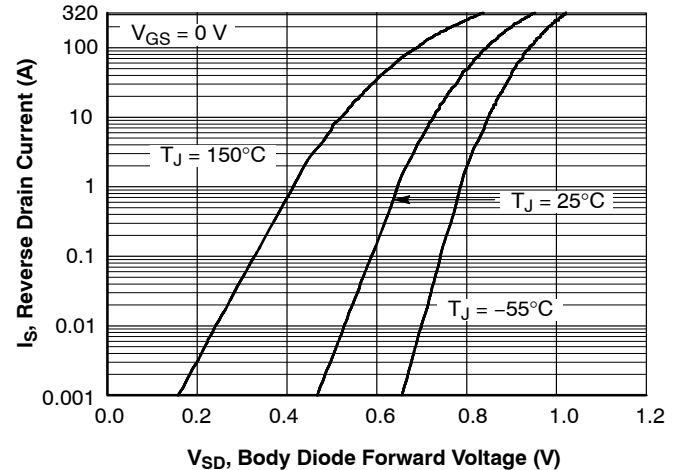


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

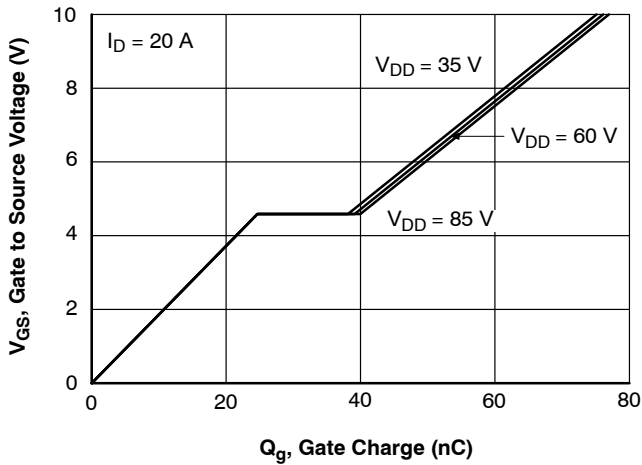


Figure 7. Gate Charge Characteristics

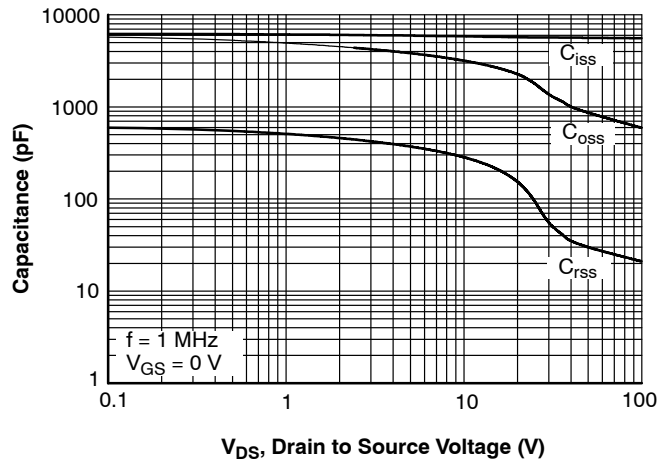


Figure 8. Capacitance vs. Drain to Source Voltage

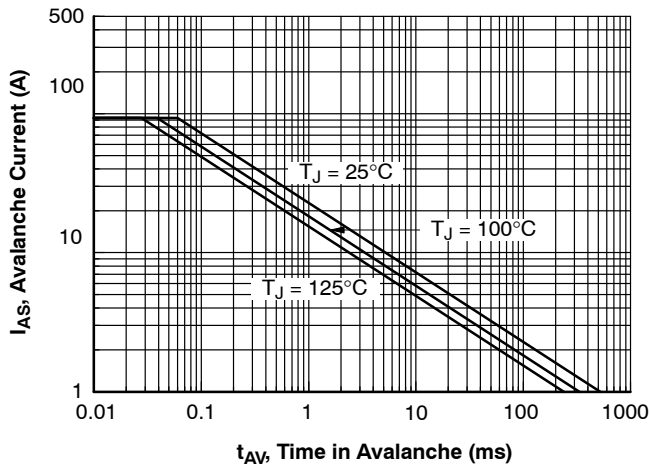


Figure 9. Unclamped Inductive Switching Capability

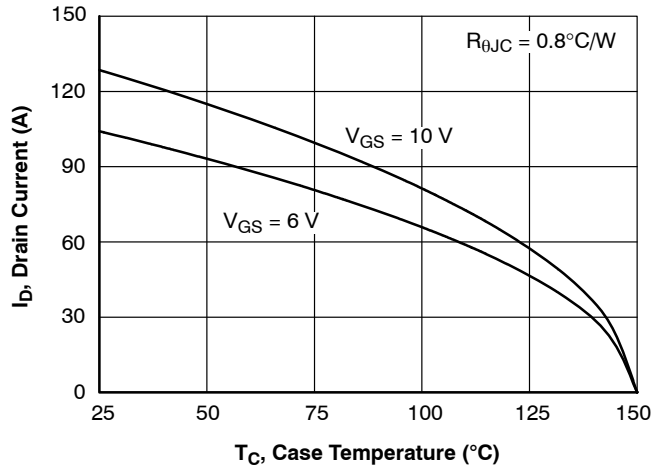


Figure 10. Maximum Continuous Drain Current vs Case Temperature

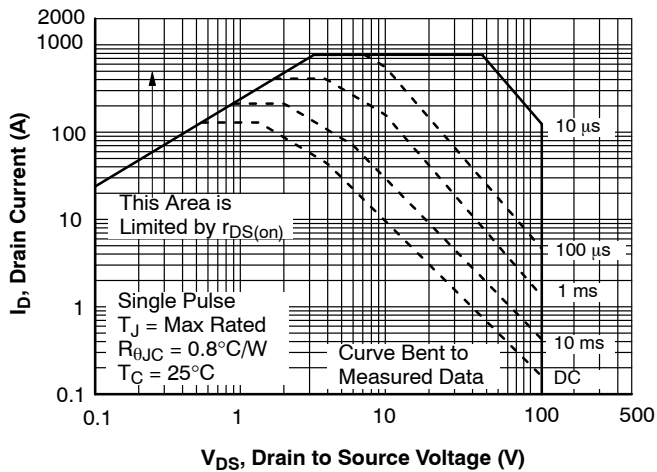


Figure 11. Forward Bias Safe Operating Area

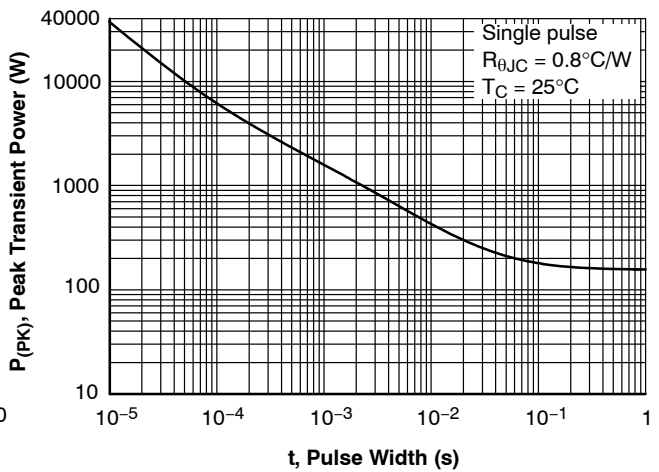


Figure 12. Single Pulse Maximum Power Dissipation

FDMT800120DC

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

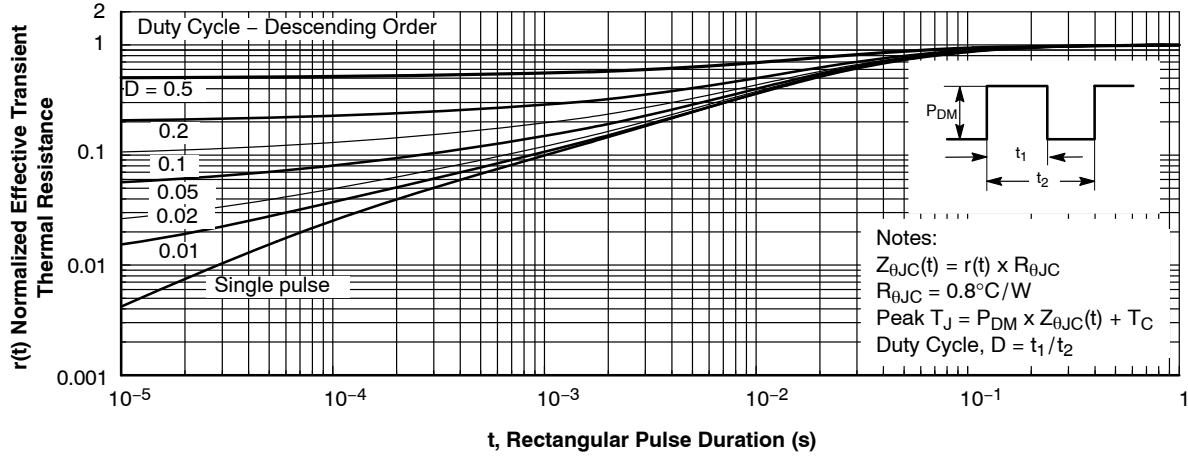


Figure 13. Junction-to-Case Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Shipping [†]
800120	FDMT800120DC	TDFNW8 8.3 × 8.4, 2P, DUAL COOL, OPTION 2	13"	13.3 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

POWERTRENCH and DUAL COOL are registered trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

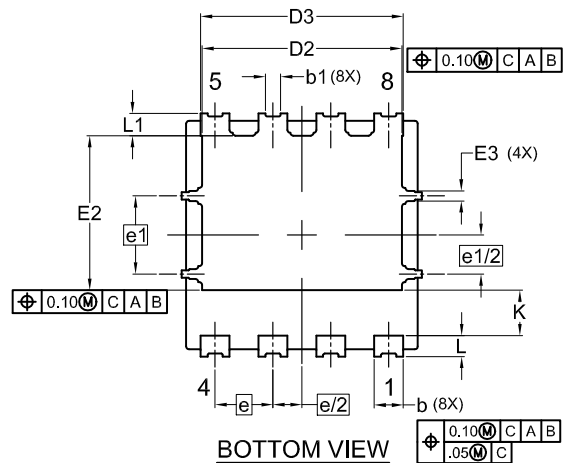
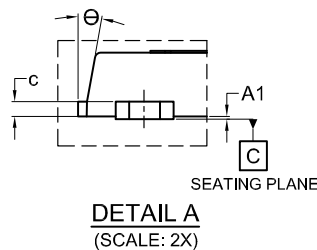
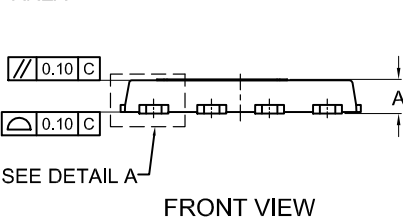
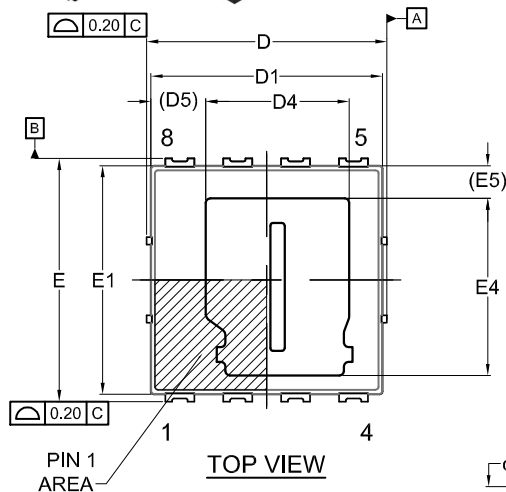
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



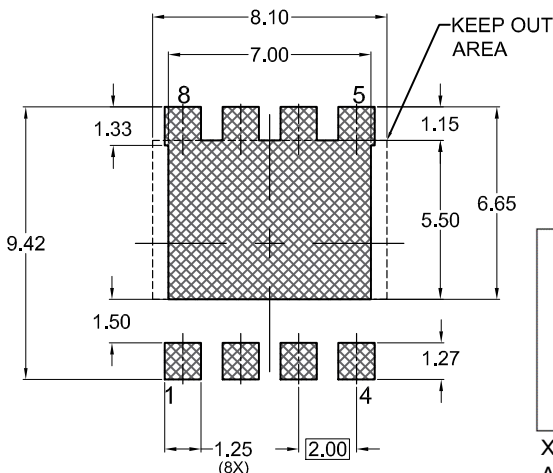
TDFNW8 8.3x8.4, 2P, DUAL COOL, OPTION 2 CASE 507AR ISSUE B

DATE 29 MAR 2021



NOTES:

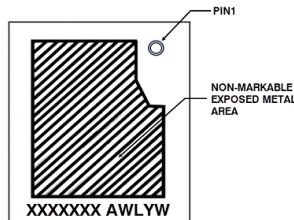
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



RECOMMENDED LAND PATTERN

(For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.)

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot Code
- Y = Year Code
- W = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.82	0.92	1.02
A1	0.00	--	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
D4	4.90	5.05	5.20
D5	1.85 REF		
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
E4	6.08	6.23	6.38
E5	1.13 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	2.70 BSC		
e1/2	1.35 BSC		
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
θ	0°	--	12°

DOCUMENT NUMBER:	98AON95711G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TDFNW8 8.3x8.4, 2P, DUAL COOL, OPTION 2	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales