- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 10 ns at 5 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down-Mode Operation**
- **Dual 4-Bit Binary Counters With Individual Clocks**
- **Direct Clear for Each 4-Bit Counter**
- **Can Significantly Improve System Densities by Reducing Counter Package Count by 50 Percent**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

SN54LV393A . . . J OR W PACKAGE
SN74LV393A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)

Pin			Pin
$\overline{1CLK}$	1	14	V_{CC}
1CLR	2	13	$\overline{2CLK}$
$1Q_A$	3	12	2CLR
$1Q_B$	4	11	$2Q_A$
$1Q_C$	5	10	$2Q_B$
$1Q_D$	6	9	$2Q_C$
GND	7	8	$2Q_D$
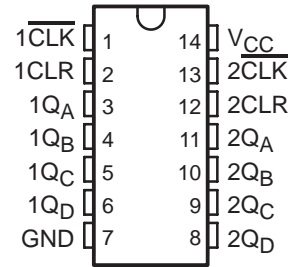
SN54LV393A . . . FK PACKAGE
(TOP VIEW)

Top pins: 1CLR (3), $\overline{1CLK}$ (2), NC (1), V_{CC} (20), $\overline{2CLK}$ (19)

$1Q_A$	4	18	2CLR
NC	5	17	NC
$1Q_B$	6	16	$2Q_A$
NC	7	15	NC
$1Q_C$	8	14	$2Q_B$

Bottom pins: $1Q_D$ (9), GND (10), NC (11), $2Q_D$ (12), $2Q_C$ (13)
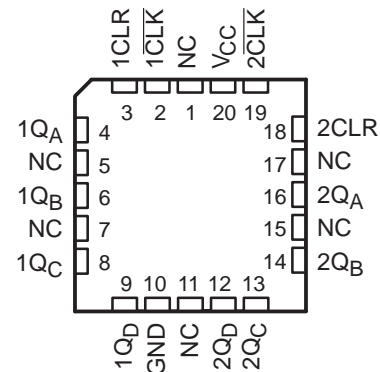
NC – No internal connection

description/ordering information

The 'LV393A devices contain eight flip-flops and additional gating to implement two individual 4-bit counters in a single package. These devices are designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – D	Tube of 50	SN74LV393AD	LV393A
		Reel of 2500	SN74LV393ADR	
	SOP – NS	Reel of 2000	SN74LV393ANSR	74LV393A
	SSOP – DB	Reel of 2000	SN74LV393ADBR	LV393A
	TSSOP – PW	Tube of 90	SN74LV393APW	LV393A
		Reel of 2000	SN74LV393APWR	
		Reel of 250	SN74LV393APWT	
	TVSOP – DGV	Reel of 2000	SN74LV393ADGVR	LV393A
−55°C to 125°C	CDIP – J	Tube of 25	SNJ54LV393AJ	SNJ54LV393AJ
	CFP – W	Tube of 150	SNJ54LV393AW	SNJ54LV393AW
	LCCC – FK	Tube of 55	SNJ54LV393AFK	SNJ54LV393AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

description/ordering informaton (continued)

These devices comprise two independent 4-bit binary counters, each having a clear (CLR) and a clock ($\overline{CLK}$) input. These devices change state on the negative-going transition of the $\overline{CLK}$ pulse. N-bit binary counters can be implemented with each package, providing the capability of divide by 256. The 'LV393A devices have parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system timing signals.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.
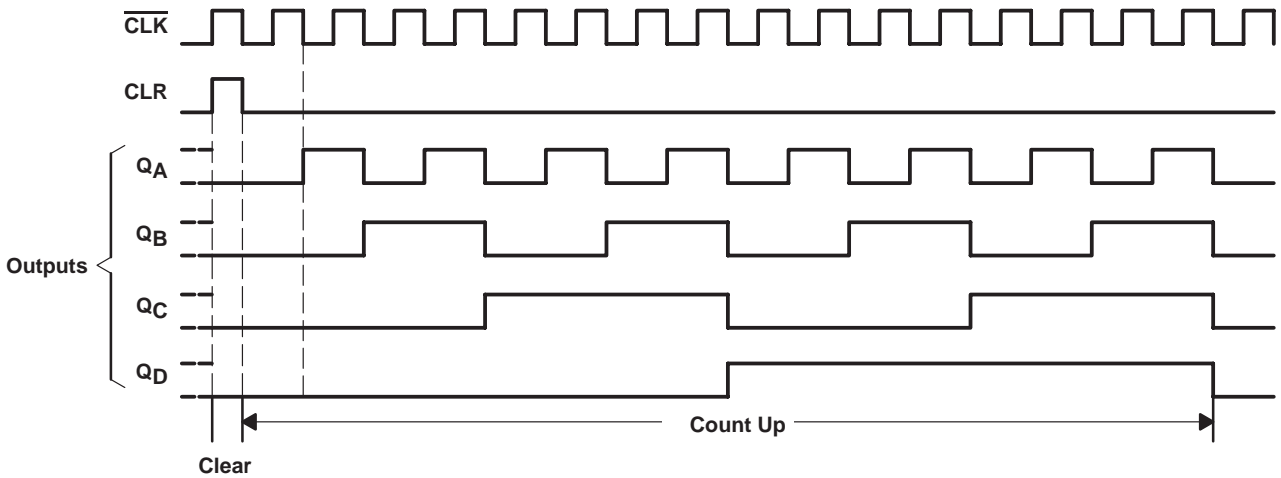
FUNCTION TABLE

INPUTS		FUNCTION
$\overline{CLK}$	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

logic diagram, each counter (positive logic)
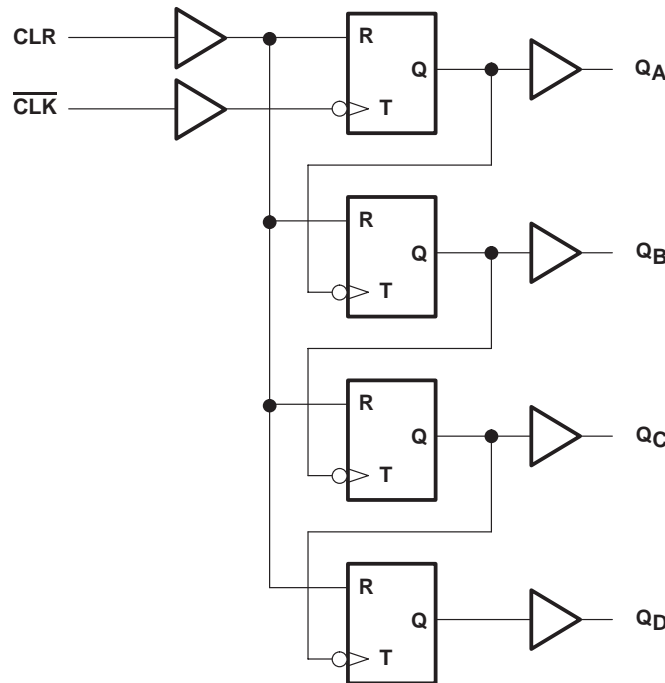
timing diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to 7 V
Output voltage range applied in high or low state, V_O (see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range applied in power-off state, V_O (see Note 1) . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$) . . . . –20 mA
Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . 86°C/W
                                                                    DB package . . . . 96°C/W
                                                                    DGV package . . . . 127°C/W
                                                                    NS package . . . . 76°C/W
                                                                    PW package . . . . 113°C/W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 7 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54LV393A, SN74LV393A
DUAL 4-BIT BINARY COUNTERS

SCLS457D – FEBRUARY 2001 – REVISED APRIL 2005

recommended operating conditions (see Note 4)

			SN54LV393A		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−6		−6	
		V_{CC} = 4.5 V to 5.5 V		−12		−12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		6		6	
		V_{CC} = 4.5 V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV393A			SN74LV393A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
	I_{OH} = −2 mA	2.3 V	2			2			
	I_{OH} = −6 mA	3 V	2.48			2.48			
	I_{OH} = −12 mA	4.5 V	3.8			3.8			
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	
	I_{OL} = 6 mA	3 V			0.44			0.44	
	I_{OL} = 12 mA	4.5 V			0.55			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	µA
C_i	V_I = V_{CC} or GND	3.3 V		1.8			1.8		pF

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV393A		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLK}$ high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	6		6		6		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV393A		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLK}$ high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV393A		SN74LV393A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{CLK}$ high or low	5		5		5		ns
		CLR high	5		5		5		
t_{su}	Setup time	CLR inactive before CLK↓	4		4		4		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V $\pm$ 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV393A		SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50*	90*		40*		40		MHz
			C_L = 50 pF	30	70		25		25		
t_{pd}	$\overline{CLK}$	Q_A	C_L = 15 pF		7.1*	17.7*	1*	20.5*	1	20.5	ns
		Q_B			8.5*	20.3*	1*	23.5*	1	23.5	
		Q_C			10*	22.5*	1*	26*	1	26	
		Q_D			11.1*	24.2*	1*	28*	1	28	
t_{PHL}	CLR	Q_n			6.7*	14.8*	1*	17*	1	17	
t_{pd}	$\overline{CLK}$	Q_A	C_L = 50 pF		9.3	21.3	1	24.5	1	24.5	ns
		Q_B			10.9	23.9	1	27.5	1	27.5	
		Q_C			12.3	26.1	1	30	1	30	
		Q_D			13.4	27.8	1	32	1	32	
t_{PHL}	CLR	Q_n			9.1	17.4	1	20	1	20	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

TEXAS INSTRUMENTS

switching characteristics over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV393A		SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75*	130*		65*		65		MHz
			C_L = 50 pF	45	105		35		35		
t_{pd}	$\overline{CLK}$	Q_A	C_L = 15 pF		5.1*	13.2*	1*	15.5*	1	15.5	ns
		Q_B			6*	15.8*	1*	18.5*	1	18.5	
		Q_C			7*	18*	1*	21*	1	21	
		Q_D			7.7*	19.7*	1*	23*	1	23	
t_{PHL}	CLR	Q_n			5.1*	12.3*	1*	14.5*	1	14.5	
t_{pd}	$\overline{CLK}$	Q_A	C_L = 50 pF		6.7	16.7	1	19	1	19	ns
		Q_B			7.8	19.3	1	22	1	22	
		Q_C			8.7	21.5	1	24.5	1	24.5	
		Q_D			9.5	23.2	1	26.5	1	26.5	
t_{PHL}	CLR	Q_n			6.8	15.8	1	18	1	18	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV393A		SN74LV393A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	125*	185*		105*		105		MHz
			C_L = 50 pF	85	150		75		75		
t_{pd}	$\overline{CLK}$	Q_A	C_L = 15 pF		3.7*	8.5*	1*	10*	1	10	ns
		Q_B			4.3*	9.8*	1*	11.5*	1	11.5	
		Q_C			4.9*	11.2*	1*	13*	1	13	
		Q_D			5.3*	12.5*	1*	14.5*	1	14.5	
t_{PHL}	CLR	Q_n			3.9*	8.1*	1*	9.5*	1	9.5	
t_{pd}	$\overline{CLK}$	Q_A	C_L = 50 pF		4.9	10.5	1	12	1	12	ns
		Q_B			5.6	11.8	1	13.5	1	13.5	
		Q_C			6.2	13.2	1	15	1	15	
		Q_D			6.6	14.5	1	16.5	1	16.5	
t_{PHL}	CLR	Q_n			5.2	10.1	1	11.5	1	11.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

TEXAS INSTRUMENTS

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noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 5)

PARAMETER		SN74LV393A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.2	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.8		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5:   Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 10 MHz	3.3 V	15.2	pF
			5 V	17.3	

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

TEXAS INSTRUMENTS

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV393AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV393A	Samples
SN74LV393APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples
SN74LV393APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV393A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV393A :

- Automotive : SN74LV393A-Q1

- Enhanced Product : SN74LV393A-EP

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV393ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV393ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV393ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV393ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV393APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV393ADBR	SSOP	DB	14	2000	853.0	449.0	35.0
SN74LV393ADGVR	TVSOP	DGV	14	2000	853.0	449.0	35.0
SN74LV393ADR	SOIC	D	14	2500	853.0	449.0	35.0
SN74LV393ANSR	SO	NS	14	2000	853.0	449.0	35.0
SN74LV393APWR	TSSOP	PW	14	2000	853.0	449.0	35.0

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
         D. Falls within JEDEC: 24/48 Pins – MO-153
                            14/16/20/56 Pins – MO-194

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
⟨C⟩

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⟨D⟩

1   7

Pin 1
Index Area

0.050 (1,27)   0.020 (0,51)
                    0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max   0.010 (0,25)
                                0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
       ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
           not exceed 0.006 (0,15) each side.
       ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AB.

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

14x1,50

12x1,27

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
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PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0,65   0,30 / 0,19   ⊕ 0,10 Ⓜ

14   8

△D△ 4,50 / 4,30   6,60 / 6,20

1   7

5,10 / 4,90
△C△

0,15 NOM
Gage Plane
0,25
0°−8°
0,75 / 0,50

1,20 MAX   0,15 / 0,05

Seating Plane
◯ 0,10

4040064−3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        △C△ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        △D△ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

TEXAS INSTRUMENTS
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PW (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Stencil Openings
(Note D)

14x0,30

12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284−2/G 08/15

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DB (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
            B. This drawing is subject to change without notice.
            C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
            D. Falls within JEDEC MO-150

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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