TPS3809x 3-Pin Supply Voltage Supervisors

1 Features

- 3-pin SOT-23 package
- Supply current of 9 µA (typical)
- Precision supply voltage monitor
  2.5 V, 3 V, 3.3 V, 5 V
- Pin-for-pin compatible with MAX 809
- Temperature range: –40°C to +85°C

2 Applications

- Factory automation
- Wireless speakers
- Motor drives
- Servers
- Appliances
- Electricity meters
- Building automation

3 Description

The TPS3809 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems. The newer TLV809E device is an alternative with the same pins, functions and electrical parameters.

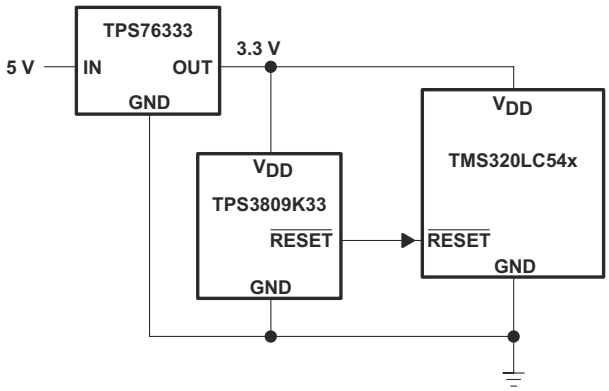
During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage V_{IT}. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d(typ)}$ = 200 ms, starts after V_{DD} has risen above the threshold voltage V_{IT}. When the supply voltage drops below the threshold voltage V_{IT}, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed sense-threshold voltage V_{IT} set by an internal voltage divider.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 3-pin SOT-23. The TPS3809 devices are characterized for operation over a temperature range of –40°C to 85°C.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPS3809	SOT-23 (3), DBV	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

Table of Contents

4 Revision History

Changes from Revision C (October 2013) to Revision D (January 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added new sentence regarding the new TLV809E to the *Description* section	1
• Added the pinout and pin function table	4
• Changed VDD from 7 to 6.5 in *Absolute Maximum Ratings*	5
• Changed V_{OL} @ 500µA from 0.2 to 0.3V and corrected header of the table from TPS3800-xx, TPS3801-xx, TPS3802-xx to TPS3809xx in *Electrical Characteristics*	5
• Changed t_w pulse duration from 3 to 10µs in *Timing Requirements*	6
• Changed t_{PHL} from 1 to 10µs in *Switching Characteristics*	6

Changes from Revision B (July 2012) to Revision C (October 2013)	Page
• Changed front page and page flow to match current standard look and feel	1
• Changed "Operating junction temperature range" to "Operating free-air temperature range" in Absolute Maximum Ratings (typo)	5

Changes from Revision A (October 2010) to Revision B (July 2012)	Page
• Changed the Pull-up resistor value, $\overline{\text{RESET}}$ To: $\overline{\text{RESET}}$ current sink during startup in the Recommended Operating Conditions Table	5

Changes from Revision * (August 1999) to Revision A (October 2010)	Page
• Added Pull-up resistor value, $\overline{\text{RESET}}$ to the Recommended Operating Conditions Table	5

5 Device Comparison

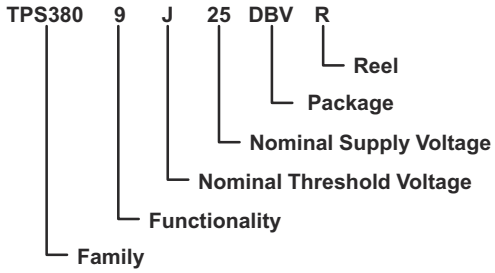
Table 5-1. Device Comparison Table

T_A	DEVICE NAME		THRESHOLD VOLTAGE	MARKING
–40°C to 85°C	TPS3809J25DBVR	TPS3809J25DBVT	2.25 V	PCZI
	TPS3809L30DBVR	TPS3809L30DBVT	2.64 V	PDAI
	TPS3809K33DBVR	TPS3809K33DBVT	2.93 V	PDBI
	TPS3809I50DBVR	TPS3809I50DBVT	4.55 V	PDCI

FUNCTION/TRUTH TABLE, TPS3809

$V_{DD}>V_{IT}$	$\overline{RESET}$
0	L
1	H

ORDERING INFORMATION



6 Pin Configuration and Functions

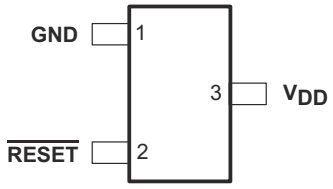


Figure 6-1. Pin configuration

Table 6-1. Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
GND	1	-	This pin should be connected to ground with a low-impedance connection.
$\overline{\text{RESET}}$	2	O	$\overline{\text{RESET}}$ is an active low signal, asserting when V_{DD} is below the threshold voltage. When V_{DD} rises above V_{IT}, there is a delay time (t_d) until $\overline{\text{RESET}}$ deasserts. $\overline{\text{RESET}}$ is a push-pull output stage.
VDD	3	-	Supply voltage pin. A 0.1-µF ceramic capacitor from this pin to ground is recommended to improve stability of the threshold voltage

7 Specifications

7.1 Absolute Maximum Ratings (1) (2)

Over operating free-air temperature range (unless otherwise noted).

	UNIT
Supply voltage, V_{DD}	6.5 V
All other pins	–0.3 V to 6.5 V
Maximum low-output current, I_{OL}	5 mA
Maximum high-output current, I_{OH}	–5 mA
Input-clamp current, I_{IK} (V_I < 0 or V_I > V_{DD})	±20 mA
Output-clamp current, I_{OK} (V_O < 0 or V_O > V_{DD})	±20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation, the device should not be operated at 6.5 V for more than t = 1000h continuously.

7.2 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
$\overline{\text{RESET}}$ current sink during startup		50	µA
Operating free-air temperature range, T_A	–40	+85	°C

7.3 Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A < 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

7.4 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	TPS3809xx			UNIT
				MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{DD} = 2.5 V to 6 V I_{OH} = –500 µA	V_{DD} –0.2			V
			V_{DD} = 3.3 V I_{OH} = –2 mA	V_{DD} –0.4			
			V_{DD} = 6 V I_{OH} = –4 mA	V_{DD} –0.4			
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA			0.3	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power-up reset voltage(1)		V_{DD} ≥ 1.1 V, I_{OL} = 50 µA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage(2)	TPS3809J25	T_A = –40°C to 85°C	2.2	2.25	2.3	V
		TPS3809L30		2.58	2.64	2.7	
		TPS3809K33		2.87	2.93	2.99	
		TPS3809I50		4.45	4.55	4.65	
V_{hys}	Threshold hysteresis	TPS3809J25			30		mV
		TPS3809L30			35		
		TPS3809K33			40		
		TPS3809I50			60		

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	TPS3809xx			UNIT
				MIN	TYP	MAX	
I_{DD}	Supply current		V_{DD} = 2 V, output unconnected		9	12	µA
			V_{DD} = 6 V, output unconnected		20	25	
C_i	Input capacitance		V_I = 0 V to V_{DD}		5		pF

(1) The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,\ VDD} \geq 15$ µs/V.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (0.1-µF ceramic) should be placed near the supply terminals.

7.5 Timing Requirements

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

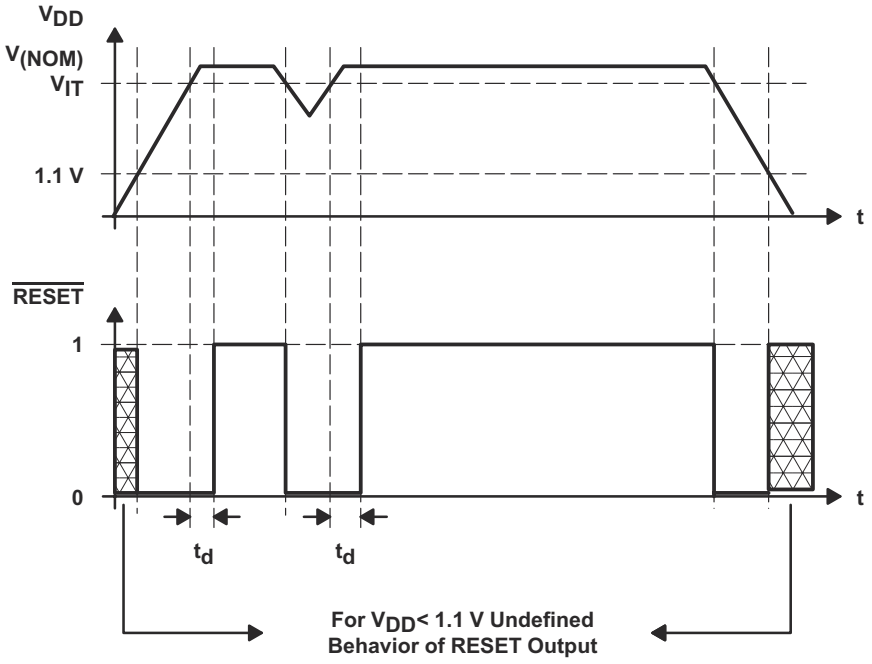
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	at V_{DD}	$V_{DD} = V_{IT-} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V	10			µs

7.6 Switching Characteristics

at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT-} + 0.2$ V, See timing diagram	120	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{\text{RESET}}$ delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V		10		µs

7.7 Timing Diagram



7.8 Typical Characteristics

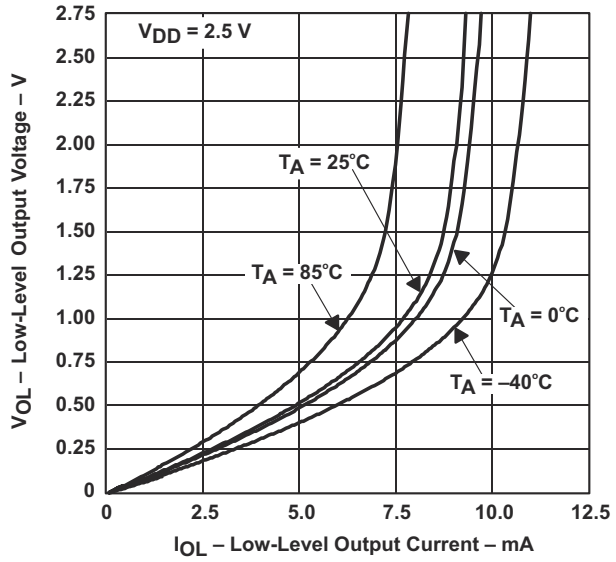


Figure 7-1. LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

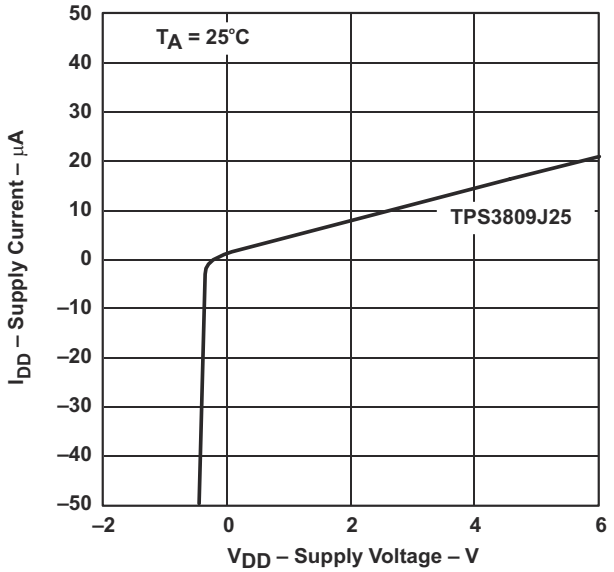


Figure 7-2. SUPPLY CURRENT vs SUPPLY VOLTAGE

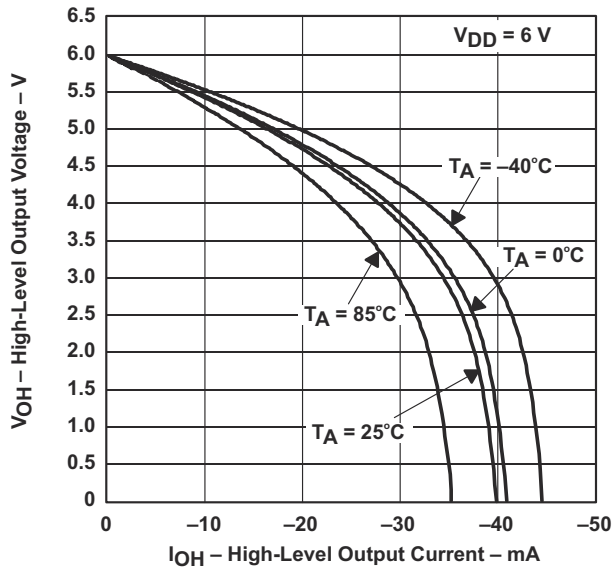


Figure 7-3. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT at V_{DD}=6V

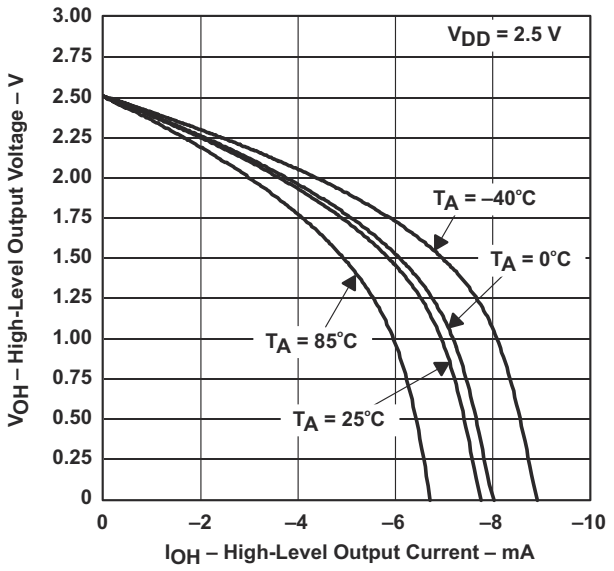


Figure 7-4. HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT at V_{DD}=2.5V

7.8 Typical Characteristics (continued)

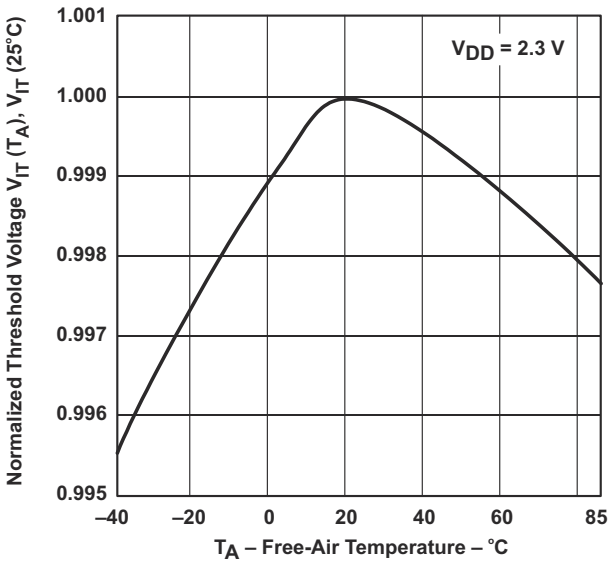
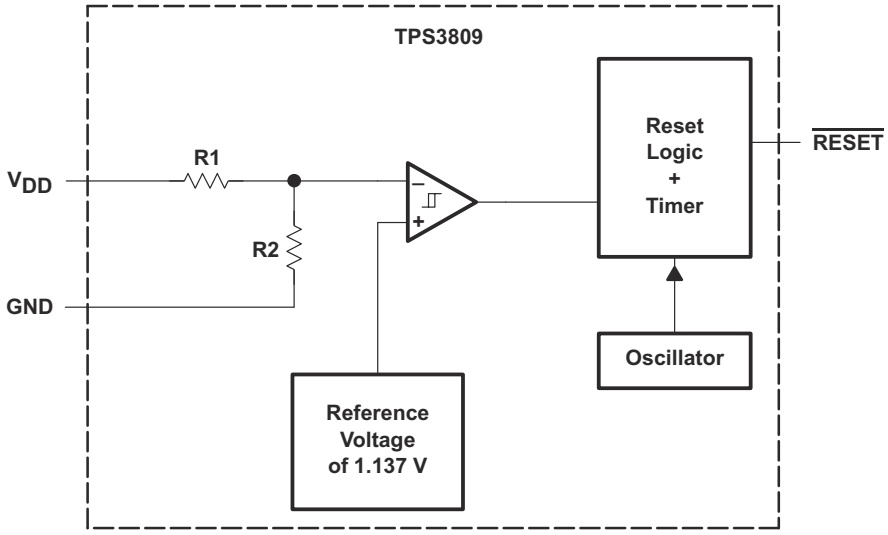


Figure 7-5. NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}=2.3V

8 Detailed Description



9 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3809I50DBVR	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDCI	Samples
TPS3809I50DBVRG4	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDCI	Samples
TPS3809I50DBVT	ACTIVE	SOT-23	DBV	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDCI	Samples
TPS3809J25DBVR	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCZI	Samples
TPS3809J25DBVT	ACTIVE	SOT-23	DBV	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCZI	Samples
TPS3809J25DBVTG4	ACTIVE	SOT-23	DBV	3	250	TBD	Call TI	Call TI	-40 to 85		Samples
TPS3809K33DBVR	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDBI	Samples
TPS3809K33DBVRG4	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDBI	Samples
TPS3809K33DBVT	ACTIVE	SOT-23	DBV	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDBI	Samples
TPS3809K33DBVTG4	ACTIVE	SOT-23	DBV	3	250	TBD	Call TI	Call TI	-40 to 85		Samples
TPS3809L30DBVR	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDAI	Samples
TPS3809L30DBVRG4	ACTIVE	SOT-23	DBV	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDAI	Samples
TPS3809L30DBVT	ACTIVE	SOT-23	DBV	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PDAI	Samples
TPS3809L30DBVTG4	ACTIVE	SOT-23	DBV	3	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3809 :

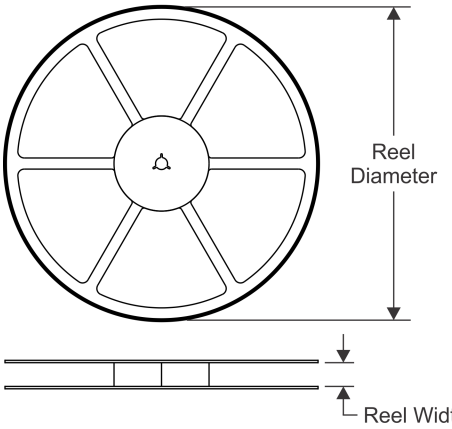
- Automotive : TPS3809-Q1
- Enhanced Product : TPS3809-EP

NOTE: Qualified Version Definitions:

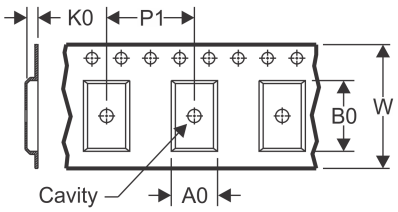
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

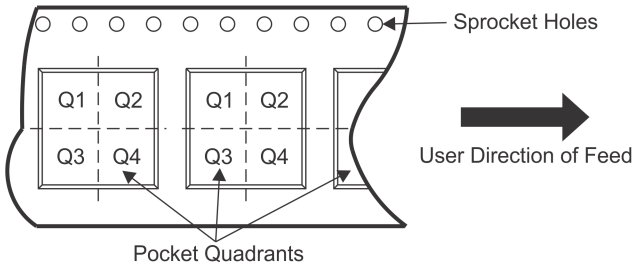


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

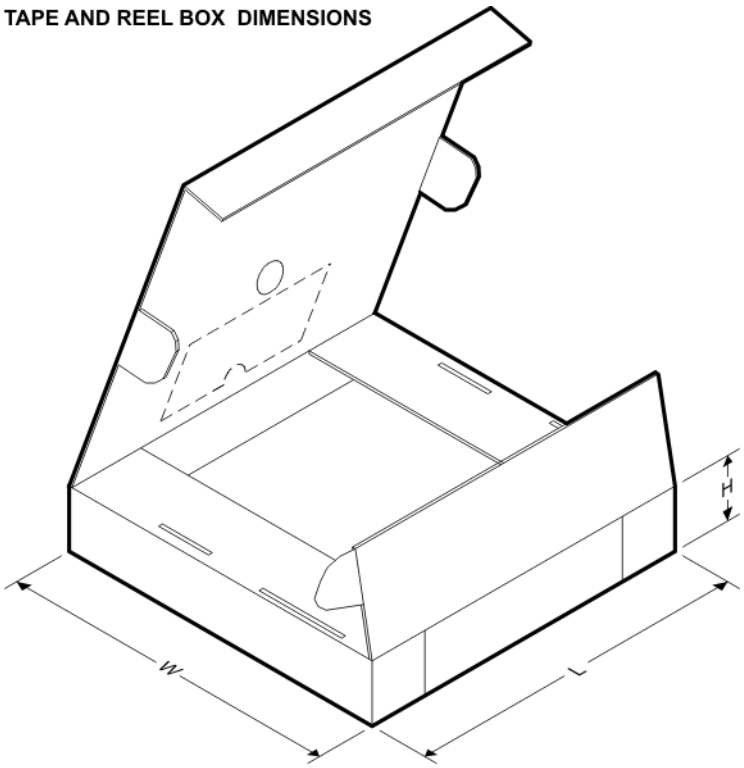
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3809I50DBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809I50DBVT	SOT-23	DBV	3	250	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809J25DBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809J25DBVT	SOT-23	DBV	3	250	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809K33DBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809K33DBVT	SOT-23	DBV	3	250	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809L30DBVR	SOT-23	DBV	3	3000	178.0	9.0	3.3	3.2	1.47	4.0	8.0	Q3
TPS3809L30DBVT	SOT-23	DBV	3	250	178.0	8.4	3.3	3.2	1.47	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

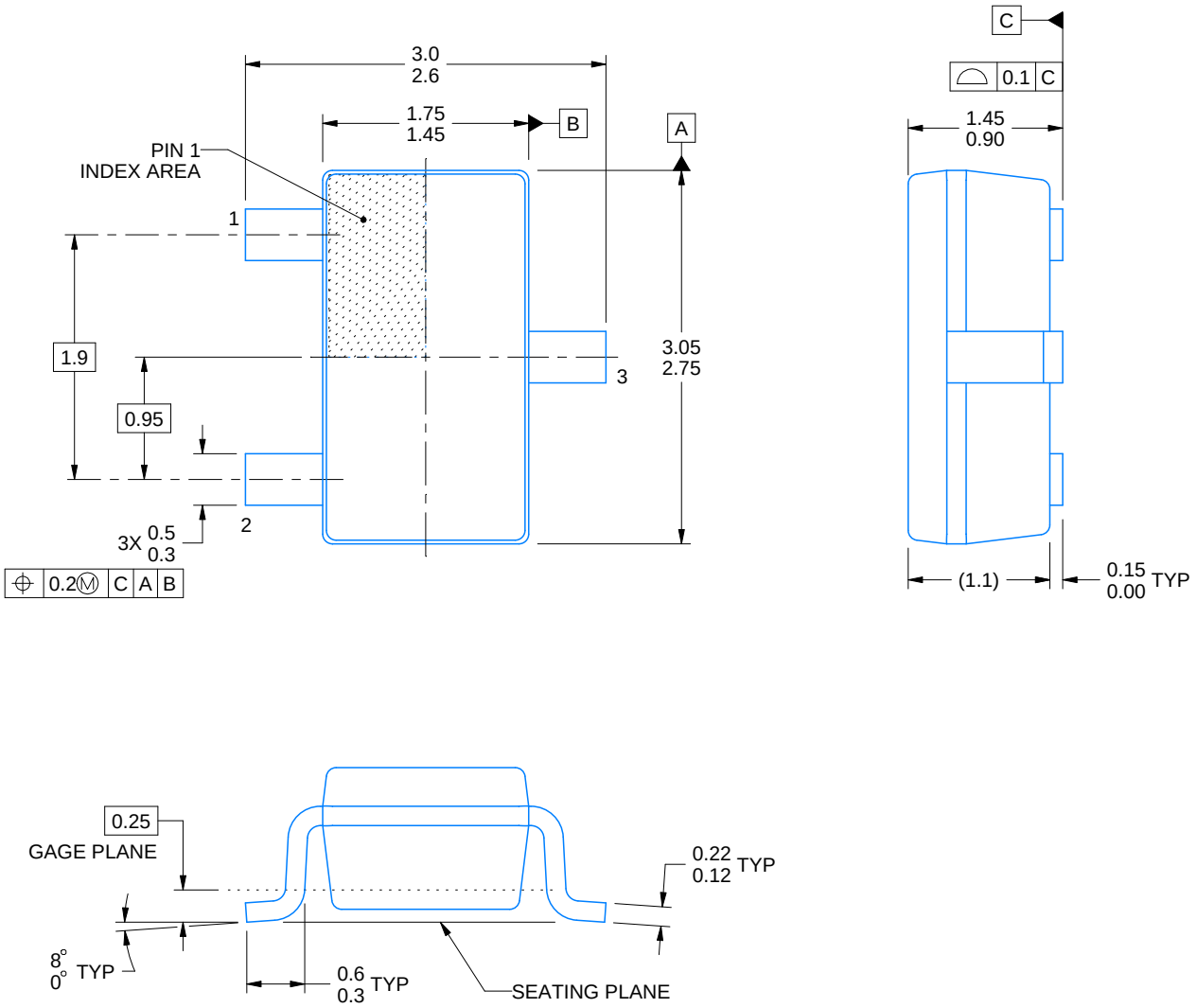
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3809I50DBVR	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809I50DBVT	SOT-23	DBV	3	250	180.0	180.0	18.0
TPS3809J25DBVR	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809J25DBVT	SOT-23	DBV	3	250	180.0	180.0	18.0
TPS3809K33DBVR	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809K33DBVT	SOT-23	DBV	3	250	180.0	180.0	18.0
TPS3809L30DBVR	SOT-23	DBV	3	3000	180.0	180.0	18.0
TPS3809L30DBVT	SOT-23	DBV	3	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0003A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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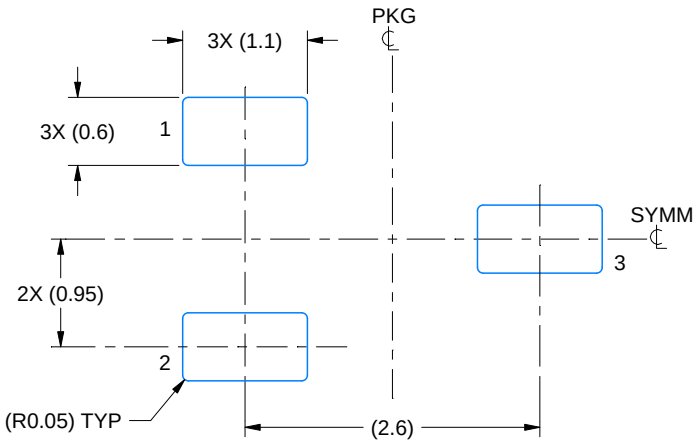
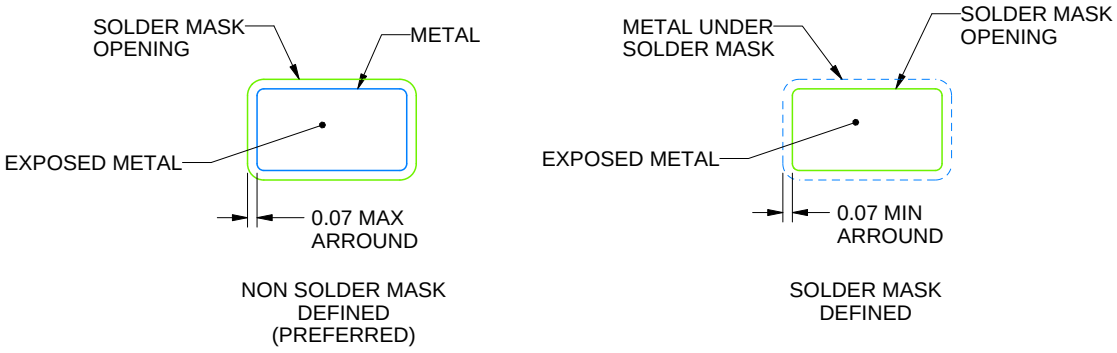
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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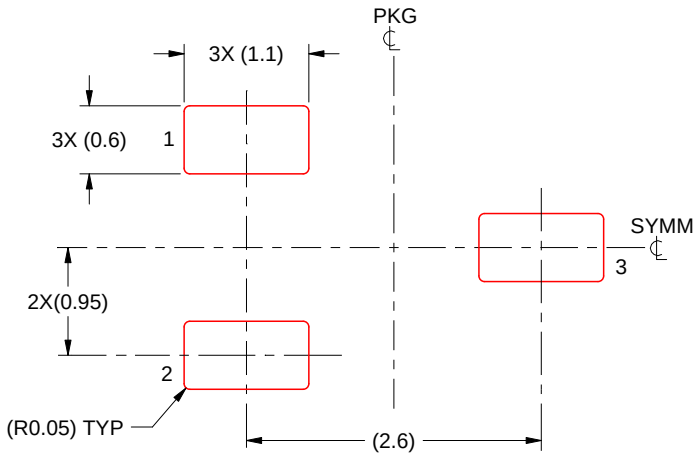
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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